19-2661; Rev 1; 9/05

MAXIM

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

General Description

The MAX1992/MAX1993 pulse-width modulation (PWM) controllers provide high-efficiency, excellent transient response, and high DC output accuracy. The devices step down high-voltage batteries to generate low-voltage CPU core or chipset/RAM supplies in notebook computers.

Maxim's proprietary Quick-PWM™ quick-response, constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients, while maintaining a relatively constant switching frequency. Efficiency is enhanced by the ability to drive very large synchronous-rectifier MOSFETs. Current sensing to ensure reliable overload and inductor saturation protection is available using an external current-sense resistor in series with the output. Alternatively, the controller can sense the current across the synchronous rectifier alone or use lossless inductor sensing for lowest power dissipation.

Single-stage buck conversion allows the MAX1992/MAX1993 to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down from another system supply rail instead of the battery) at the maximum switching frequency allows the minimum possible physical size.

The MAX1992 powers the CPU core, chipset, DRAM, or other supply rails as low as 0.7V. The MAX1993 powers chipsets and graphics processor cores, which require dynamically adjustable output voltages. The MAX1993 provides a tracking input that can be used for active termination buses. The MAX1992/MAX1993 are available in a 24-pin thin QFN package with optional overvoltage and undervoltage protection.

For dual step-down PWM controllers with inductor saturation protection, external reference input voltage, and dynamically selectable output voltages, refer to the MAX1540/MAX1541 data sheet.

Applications

Notebook Computers

Core/IO Supplies as Low as 0.7V

1.8V and 2.5V Supplies

DDR Memory Termination (MAX1993)

Active Termination Buses (MAX1993)

CPU/Chipset/GPU with Dynamic Voltage Cores (MAX1993)

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

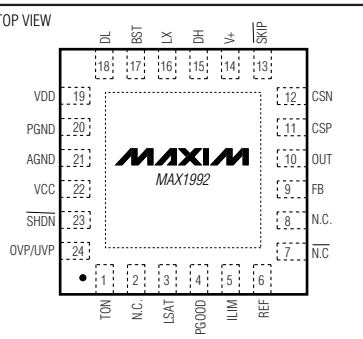
- ♦ **Inductor Saturation Protection**
- ♦ **Accurate Current Limit**
- ♦ **Ultra-High Efficiency**
- ♦ **Quick-PWM with 100ns Load-Step Response**
- ♦ **MAX1992**
  - **1.8V/2.5V Fixed or 0.7V to 5.5V Adjustable Output Range**
- ♦ **MAX1993**
  - **External Reference Input**
  - **Dynamically Selectable Output Voltage (0.7V to 5.5V)**
  - **Optional Power-Good and Fault Blanking During Transitions**
- ♦ **±1% V_{OUT} Accuracy Over Line and Load**
- ♦ **2V to 28V Battery Input Range (V_{IN})**
- ♦ **200/300/450/600kHz Switching Frequency**
- ♦ **Overvoltage/Undervoltage Protection Option**
- ♦ **1.7ms Digital Soft-Start**
- ♦ **Drives Large Synchronous Rectifier FETs**
- ♦ **2V ±0.7% Reference Output**
- ♦ **Power-Good Window Comparator**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1992ETG	-40°C to +85°C	24 Thin QFN 4mm × 4mm
MAX1992ETG+	-40°C to +85°C	24 Thin QFN 4mm × 4mm
MAX1993ETG	-40°C to +85°C	24 Thin QFN 4mm × 4mm
MAX1993ETG+	-40°C to +85°C	24 Thin QFN 4mm × 4mm

+ Denotes lead-free package.

Pin Configurations



THIN QFN
4mm x 4mm

A "+" SIGN WILL REPLACE THE FIRST PIN INDICATOR ON LEAD-FREE PACKAGES.

Pin Configurations continued at end of data sheet.

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ to AGND .....-0.3V to +30V
V_{CC} to AGND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
PGOOD, ILIM, $\overline{SKIP}$, $\overline{SHDN}$ to AGND .....-0.3V to +6V
REFIN, FB, CSP to AGND .....-0.3V to +6V
GATE, OD to GND (MAX1993 only) .....-0.3V to +6V
TON, OVP/UVP, LSAT to AGND .....-0.3V to (V_{CC} + 0.3V)
REF, OUT to AGND .....-0.3V to (V_{CC} + 0.3V)
FBLANK to GND (MAX1993 only) .....-0.3V to (V_{CC} + 0.3V)
DL to PGND .....-0.3V to (V_{DD} + 0.3V)
CSN to AGND .....-2V to +30V
DH to LX .....-0.3V to (BST + 0.3V)
LX to AGND .....-2V to +30V
BST to LX .....-0.3V to +6V
AGND to PGND (MAX1992 only) .....-0.3V to +0.3V
REF Short Circuit to AGND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin 4mm x 4mm Thin QFN
(derated 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range
MAX199_ETG .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: For the MAX1993, AGND and PGND refer to a single pin designated GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{IN}	Battery voltage, V+		2		28	V
	V_{BIAS}	V_{CC}, V_{DD}		4.5		5.5	
Output Voltage Accuracy (MAX1992 Fixed)	V_{OUT}	MAX1992 V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)	FB = GND	2.475	2.5	2.525	V
			FB = V_{CC}	1.782	1.8	1.818	
Feedback Voltage Accuracy (MAX1992 Adjustable)	V_{FB}	MAX1992 V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)		0.693	0.7	0.707	V
Feedback Voltage Accuracy (MAX1993)	V_{FB}	MAX1993 V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)	REFIN = 0.35 × REF	0.693	0.7	0.707	V
			REFIN = REF	1.980	2	2.020	
Load Regulation Error		I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}			0.1		%
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			0.25		%
FB Input Bias Current	I_{FB}			-0.1		+0.1	µA
Output Adjust Range				0.7		5.5	V
OUT Input Resistance	R_{OUT}	MAX1992	FB = GND	90	190	350	kΩ
			FB = V_{CC} or adjustable	70	145	270	
		MAX1993		400	800	1400	
OUT Discharge Mode On-Resistance	$R_{DISCHARGE}$				10	25	Ω
OUT Synchronous Rectifier Discharge Mode Turn-On Level				0.2	0.3	0.4	V
Soft-Start Ramp Time	t_{SS}	Rising edge on $\overline{SHDN}$ to full current limit			1.7		ms

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time	t_{ON}	V+ = 15V, V_{OUT} = 1.5V (Note 3)	TON = GND (600kHz)	170	194	219	ns
			TON = REF (450kHz)	213	243	273	
			TON = open (300kHz)	316	352	389	
			TON = V_{CC} (200kHz)	461	516	571	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			400	500	ns
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above the regulation point, LSAT = GND			0.55	0.85	mA
		FB forced above the regulation point, V_{LSAT} > 0.5V				1	
Quiescent Supply Current (V_{DD})	I_{DD}	FB forced above the regulation point			<1	5	µA
Quiescent Supply Current (V+)	I_{V+}				25	40	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND			<1	7	µA
Shutdown Supply Current (V_{DD})		$\overline{SHDN}$ = GND			<1	5	µA
Shutdown Supply Current (V+)		$\overline{SHDN}$ = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
REFERENCE							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	T_A = +25°C to +85°C	1.986	2	2.014	V
			T_A = 0°C to +85°C	1.983	2	2.017	
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to 50µA		-0.01		+0.01	V
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 350mV			1.95		V
REFIN Voltage Range				0.7		V_{REF}	V
REFIN Input Bias Current	I_{REFIN}				0.01	0.05	µA
FAULT DETECTION							
Overvoltage Trip Threshold		With respect to error comparator threshold, OVP/UVP = V_{CC}		12	16	20	%
Overvoltage Fault Propagation Delay	t_{OVP}	FB forced 2% above trip threshold			10		µs
Output Undervoltage Protection Trip Threshold		With respect to error comparator threshold, OVP/UVP = V_{CC}		65	70	75	%
Output Undervoltage Protection Blanking Time	t_{BLANK}	From rising edge of $\overline{SHDN}$		10		35	ms
Output Undervoltage Fault Propagation Delay	t_{UVP}				10		µs
PGOOD Lower Trip Threshold		With respect to error comparator threshold, hysteresis = 1%		-13	-10	-7	%
PGOOD Upper Trip Threshold		With respect to error comparator threshold, hysteresis = 1%		+7	+10	+13	%
PGOOD Propagation Delay	t_{PGOOD}	FB forced 2% beyond PGOOD trip threshold			10		µs

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Output Low Voltage		I_{SINK} = 4mA				0.3	V
PGOOD Leakage Current	I_{PGOOD}	FB = REF (PGOOD high impedance), PGOOD forced to 5.5V				1	µA
Fault Blanking Time	t_{FBLANK}	FBLANK = V_{CC}		120	218	320	µs
		FBLANK = open		80	140	205	
		FBLANK = REF		35	63	95	
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level hysteresis = 20mV		4.1	4.25	4.4	V
CURRENT LIMIT							
ILIM Adjustment Range				0.25		2.00	V
Current-Limit Input Range		CSP		0		2.7	V
		CSN		-0.3		+28.0	
CSP/CSN Input Current				-0.5		+0.5	µA
Valley Current-Limit Threshold (Fixed)	$V_{LIM(VAL)}$	V_{CSP} - V_{CSN}, ILIM = V_{CC}		45	50	55	mV
Valley Current-Limit Threshold (Adjustable)	$V_{LIM(VAL)}$	V_{CSP} - V_{CSN}	V_{ILIM} = 250mV	15	25	35	mV
			V_{ILIM} = 2.00V	170	200	230	
Current-Limit Threshold (Negative)	V_{NEG}	V_{CSP} - V_{CSN}, $\overline{SKIP}$ = ILIM = V_{CC}, T_A = +25°C		-75	-60	-45	mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	With respect to valley current-limit threshold, V_{CSP} - V_{CSN}, $\overline{SKIP}$ = GND, ILIM = V_{CC}			2.5		mV
Inductor Saturation Current-Limit Threshold		With respect to valley current-limit threshold, ILIM = V_{CC}	LSAT = V_{CC}	180	200	220	%
			LSAT = open	157	175	193	
			LSAT = REF	135	150	165	
ILIM Saturation Fault Sink Current	$I_{ILIM(LSAT)}$	V_{CSP} - V_{CSN} > inductor saturation current limit, 0.25V < V_{ILIM} < 2.0V		4	6	8	µA
ILIM Leakage Current		V_{CSP} - V_{CSN} < inductor saturation current limit				0.1	µA
GATE DRIVERS							
DH Gate Driver On-Resistance	R_{DH}	BST - LX forced to 5V			1.5	5	Ω
DL Gate Driver On-Resistance	R_{DL}	DL, high state			1.5	5	Ω
		DL, low state			0.6	3	
DH Gate Driver Source/Sink Current	I_{DH}	DH forced to 2.5V, BST - LX forced to 5V			1		A
DL Gate Driver Source Current	$I_{DL(SOURCE)}$	DL forced to 2.5V			1		A

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DL Gate Driver Sink Current	$I_{DL(SINK)}$	DL forced to 2.5V			3		A
Dead Time	t_{DEAD}	DL rising			35		ns
		DH rising			26		
INPUTS AND OUTPUTS							
OD On-Resistance	R_{OD}	GATE = V_{CC}			10	25	Ω
OD Leakage Current		GATE = GND, OD forced to 5.5V			1	200	nA
Logic Input Threshold		$\overline{SHDN}$, $\overline{SKIP}$, GATE rising edge, hysteresis = 225mV		1.20	1.7	2.20	V
Logic Input Current		$\overline{SHDN}$, $\overline{SKIP}$, GATE		-1		+1	µA
Dual Mode™ Threshold Voltage		MAX1992 FB	High	1.9	2.0	2.1	V
			Low	0.05	0.1	0.15	
Four-Level Input Logic Levels		TON, OVP/UVP, LSAT, FBLANK	High	V_{CC} - 0.4V			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.5	
Four-Level Logic Input Current		TON, OVP/UVP, LSAT, FBLANK forced to GND or V_{CC}		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V_{IN}	Battery voltage, V+		2	28	V
	V_{BIAS}	V_{CC}, V_{DD}		4.5	5.5	
Output Voltage Accuracy (MAX1992 Fixed)	V_{OUT}	MAX1992, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)	FB = GND	2.462	2.538	V
			FB = V_{CC}	1.773	1.827	
Feedback Voltage Accuracy (MAX1992 Adjustable)	V_{FB}	MAX1992, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)		0.689	0.711	V
Feedback Voltage Accuracy (MAX1993)	V_{FB}	MAX1993, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC} (Note 2)	REFIN = 0.35 × REF	0.689	0.711	V
			REFIN = REF	1.970	2.030	
On-Time	t_{ON}	V+ = 15V, V_{OUT} = 1.5V (Note 3)	TON = GND (600kHz)	170	219	ns
			TON = REF (450kHz)	213	273	
			TON = open (300kHz)	316	389	
			TON = V_{CC} (200kHz)	461	571	

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)		500	ns
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above the regulation point, LSAT = GND		0.85	mA
		FB forced above the regulation point, V_{LSAT} > 0.5V		1.0	
Quiescent Supply Current (V_{DD})	I_{DD}	FB forced above the regulation point		5	µA
Quiescent Supply Current (V+)	I_{V+}			40	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND		7	µA
Shutdown Supply Current (V_{DD})		$\overline{SHDN}$ = GND		5	µA
Shutdown Supply Current (V+)		$\overline{SHDN}$ = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V		5	µA
REFERENCE					
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	1.980	2.020	V
REFIN Voltage Range			0.7	V_{REF}	V
FAULT DETECTION					
Overvoltage Trip Threshold		With respect to error comparator threshold, OVP/UVP = V_{CC}	10	20	%
Output Undervoltage Protection Trip Threshold		With respect to error comparator threshold, OVP/UVP = V_{CC}	65	75	%
PGOOD Lower Trip Threshold		With respect to error comparator threshold, hysteresis = 1%	-14	-6	%
PGOOD Upper Trip Threshold		With respect to error comparator threshold, hysteresis = 1%	+6	+14	%
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level hysteresis = 20mV	4.1	4.4	V
CURRENT LIMIT					
Current-Limit Input Range		CSP	0	2.7	V
		CSN	-0.3	+28.0	
Valley Current-Limit Threshold (Fixed)	$V_{LIM(VAL)}$	V_{CSP} - V_{CSN}, ILIM = V_{CC}	35	65	mV
Valley Current-Limit Threshold (Adjustable)	$V_{LIM(VAL)}$	V_{CSP} - V_{CSN}, V_{ILIM} = 2.00V	160	240	mV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = $\overline{SHDN}$ = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUTS AND OUTPUTS						
Logic Input Threshold		$\overline{SHDN}$, $\overline{SKIP}$, GATE rising edge, hysteresis = 225mV		1.20	2.20	V
Dual Mode Threshold Voltage		MAX1992 FB	High	1.9	2.1	V
			Low	0.05	0.15	
Four-Level Input Logic Levels		TON, OVP/UVP, LSAT, FBLANK	High	V_{CC} - 0.4V		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.5	

Note 2: When the inductor is in continuous conduction, the output voltage has a DC regulation level higher than the error comparator threshold by 50% of the output ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

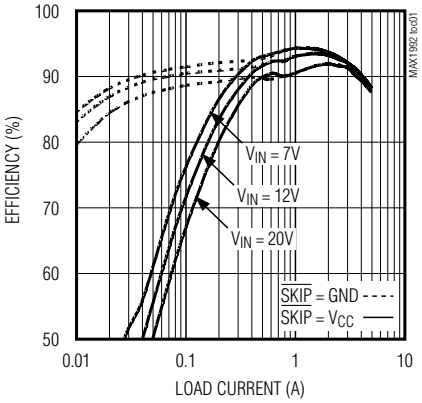
Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times can differ due to MOSFET switching speeds.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

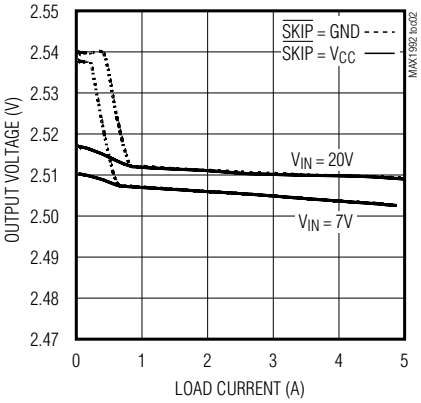
Typical Operating Characteristics

(MAX1992 Circuit of Figure 1, MAX1993 Circuit of Figure 9, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = V_{CC}, TON = open, T_A = +25°C, unless otherwise noted.)

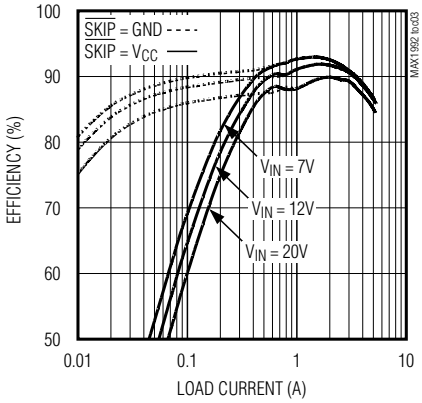
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V)



2.5V OUTPUT VOLTAGE vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.8V)

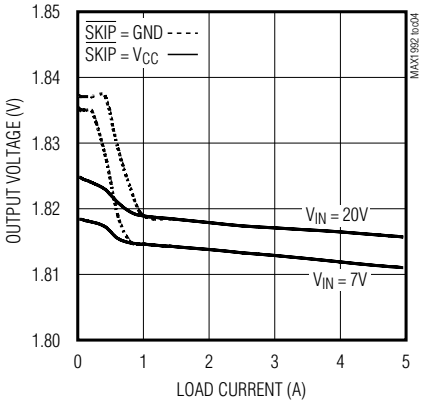


Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

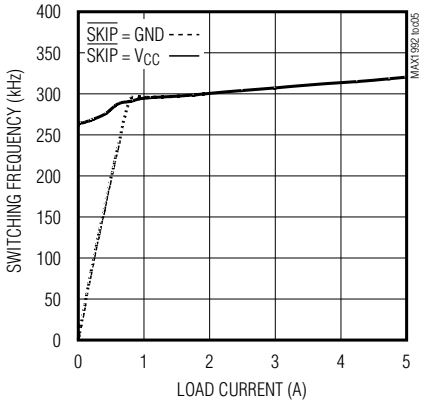
Typical Operating Characteristics (continued)

(MAX1992 Circuit of Figure 1, MAX1993 Circuit of Figure 9, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = V_{CC}, TON = open, T_A = +25°C, unless otherwise noted.)

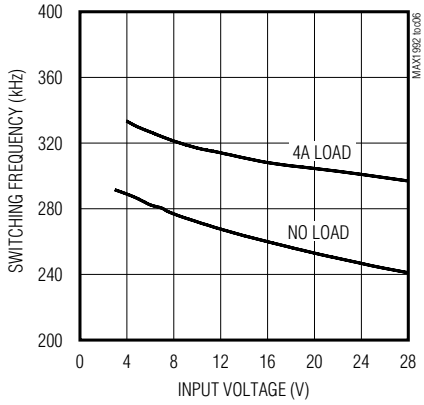
1.8V OUTPUT VOLTAGE vs. LOAD CURRENT



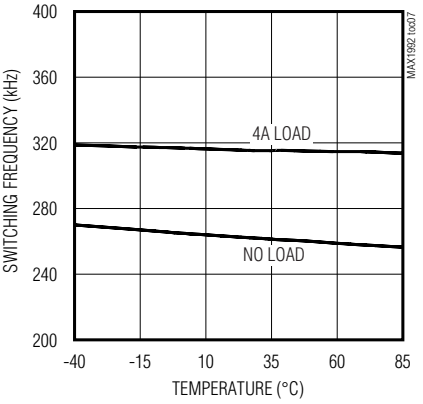
SWITCHING FREQUENCY vs. LOAD CURRENT



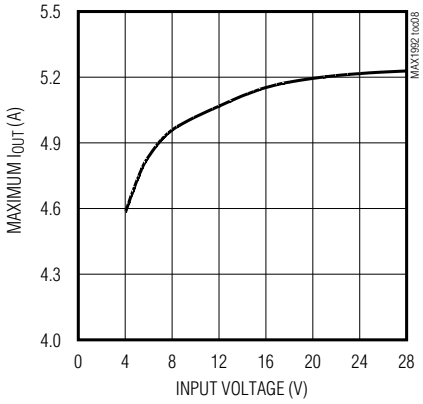
SWITCHING FREQUENCY vs. INPUT VOLTAGE



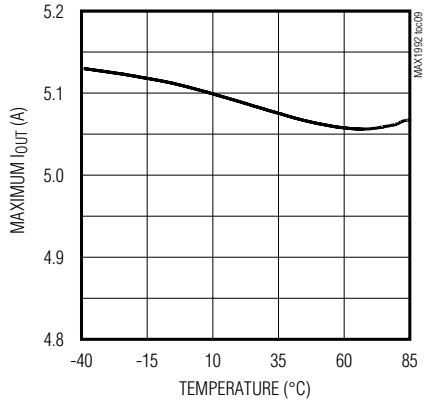
SWITCHING FREQUENCY vs. TEMPERATURE



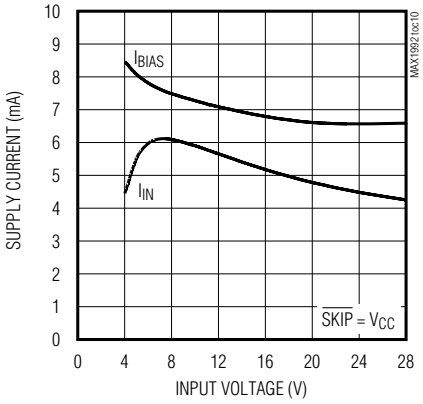
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



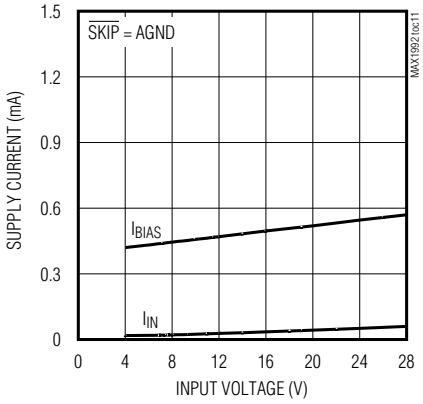
MAXIMUM OUTPUT CURRENT vs. TEMPERATURE



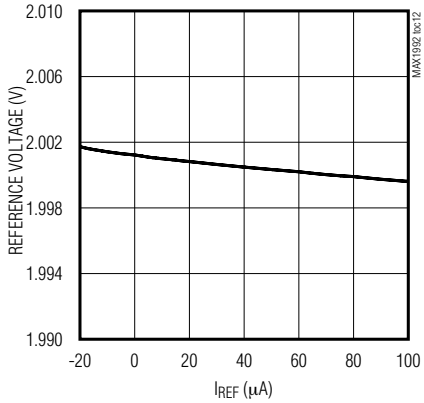
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM MODE)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



REFERENCE LOAD REGULATION

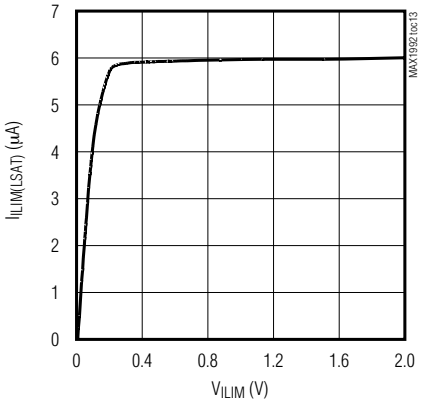


Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

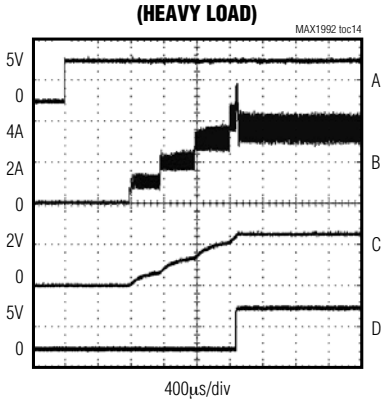
Typical Operating Characteristics (continued)

(MAX1992 Circuit of Figure 1, MAX1993 Circuit of Figure 9, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = V_{CC}, TON = open, T_A = +25°C, unless otherwise noted.)

ILIM SATURATION FAULT CURRENT vs. ILIM VOLTAGE

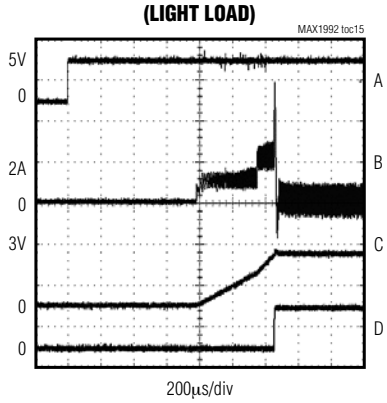


STARTUP WAVEFORMS (HEAVY LOAD)



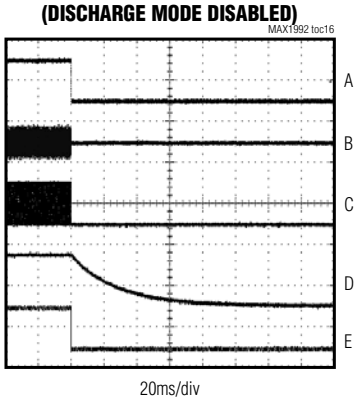
A. $\overline{SHDN}$ = 0 TO 5V; 5V/div
B. INDUCTOR CURRENT: 2A/div
C. OUTPUT VOLTAGE (V_{OUT}): 2V/div
D. PGOOD: 5V/div, 0.7Ω LOAD

STARTUP WAVEFORMS (LIGHT LOAD)



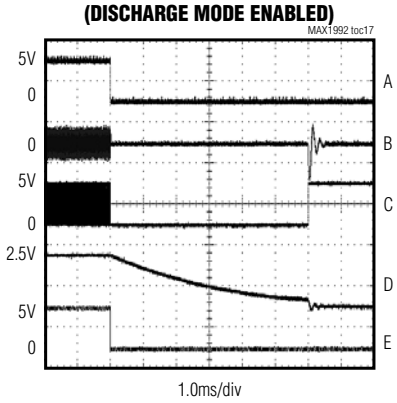
A. $\overline{SHDN}$ = 0 TO 5V; 5V/div
B. INDUCTOR CURRENT: 2A/div
C. OUTPUT VOLTAGE (V_{OUT}): 2V/div
D. PGOOD: 5V/div, 100Ω LOAD

SHUTDOWN WAVEFORMS (DISCHARGE MODE DISABLED)



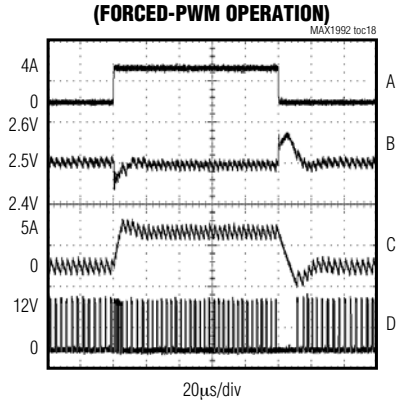
A. $\overline{SHDN}$ = 5V TO 0; 5V/div
B. INDUCTOR CURRENT: 2A/div
C. DL: 5V/div
D. OUTPUT VOLTAGE (V_{OUT}): 2V/div
E. PGOOD: 5V/div, 100Ω LOAD, OVP/UVP = OPEN OR G

SHUTDOWN WAVEFORMS (DISCHARGE MODE ENABLED)



A. $\overline{SHDN}$ = 5V TO 0; 5V/div
B. INDUCTOR CURRENT: 2A/div
C. DL: 5V/div
D. OUTPUT VOLTAGE (V_{OUT}): 2V/div
E. PGOOD: 5V/div, 100Ω LOAD, OVP/UVP = V_{CC} OR REF

LOAD TRANSIENT (FORCED-PWM OPERATION)



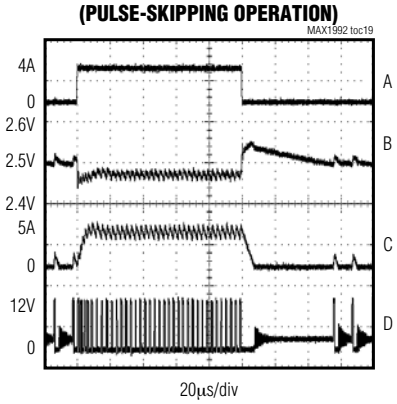
A. LOAD: I_{OUT} = 0.2A TO 4A; 5A/div
B. 2.5V OUTPUT: 100mV/div
C. INDUCTOR CURRENT: 5A/div
D. LX: 10V/div, $\overline{SKIP}$ = V_{CC}

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Typical Operating Characteristics (continued)

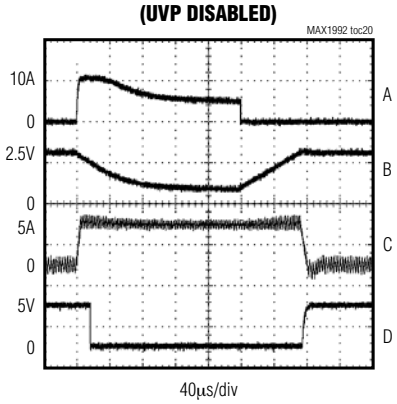
(MAX1992 Circuit of Figure 1, MAX1993 Circuit of Figure 9, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = V_{CC}, TON = open, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT (PULSE-SKIPPING OPERATION)



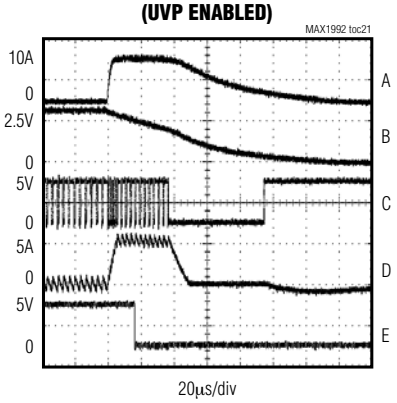
A. LOAD: I_{OUT} = 0.2A TO 4A; 5A/div
B. 2.5V OUTPUT: 100mV/div
C. INDUCTOR CURRENT: 5A/div
D. LX: 10V/div, $\overline{SKIP}$ = GND

OUTPUT OVERLOAD WAVEFORMS (UVP DISABLED)



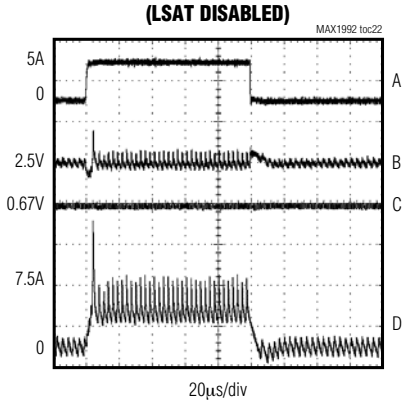
A. LOAD CURRENT (0 TO 250mΩ): 10A/div
B. 2.5V OUTPUT: 2V/div
C. INDUCTOR CURRENT: 5A/div
D. PGOOD: 5V/div, OVP/UVP = OPEN OR GND

OUTPUT OVERLOAD WAVEFORMS (UVP ENABLED)



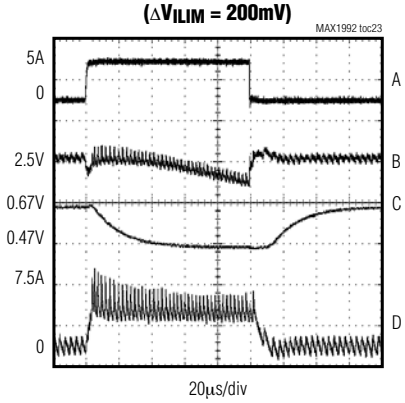
A. LOAD CURRENT (0 TO 250mΩ): 10A/div
B. 2.5V OUTPUT: 2V/div
C. DL: 5V/div
D. INDUCTOR CURRENT: 5A/div
E. PGOOD: 5V/div, OVP/UVP = V_{CC} OR REF

INDUCTOR SATURATION PROTECTION (LSAT DISABLED)



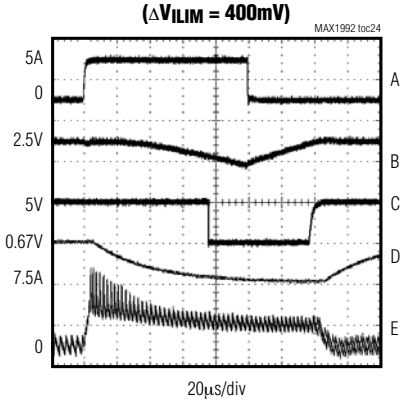
A. LOAD CURRENT: I_{OUT} = 0 TO 5A; 5A/div
B. 2.5V OUTPUT: 200mV/div
C. V_{ILIM}: 100mV/div
D. INDUCTOR CURRENT: 5A/div;
LSAT = AGND; L = 3.3µH, 3.5A

INDUCTOR SATURATION PROTECTION (ΔV_{ILIM} = 200mV)



A. LOAD CURRENT: I_{OUT} = 0 TO 5A; 5A/div
B. 2.5V OUTPUT: 200mV/div
C. V_{ILIM}: 200mV/div
D. INDUCTOR CURRENT: 5A/div,
LSAT = REF; L = 3.3µH, 3.5A

INDUCTOR SATURATION PROTECTION (ΔV_{ILIM} = 400mV)



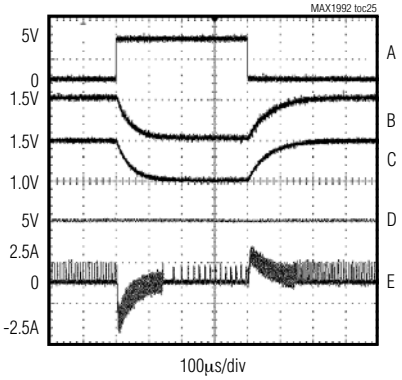
A. LOAD CURRENT: I_{OUT} = 0 TO 5A; 5A/div
B. 2.5V OUTPUT: 1V/div
C. PGOOD: 5V/div
D. V_{ILIM}: 400mV/div
E. INDUCTOR CURRENT: 5A/div,
LSAT = REF; L = 3.3µH, 3.5A

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Typical Operating Characteristics (continued)

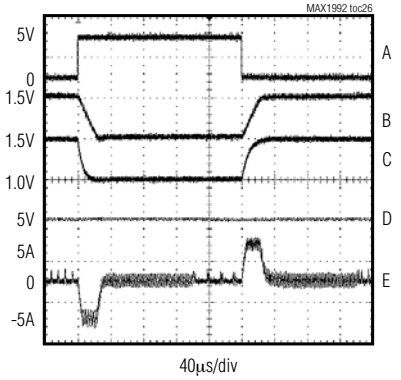
(MAX1992 Circuit of Figure 1, MAX1993 Circuit of Figure 9, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = V_{CC}, TON = open, T_A = +25°C, unless otherwise noted.)

MAX1993 DYNAMIC OUTPUT VOLTAGE TRANSITION (C_{REFIN} = 1nF)



A. V_{GATE} = 0 TO 5V; 5V/div
B. OUTPUT = 1.5V TO 1.0V; 0.5V/div
C. V_{REFIN}: 0.5V/div
D. PGOOD: 5V/div
E. INDUCTOR CURRENT: 2.5A/div
100mA LOAD, $\overline{SKIP}$ = GND, CIRCUIT OF FIGURE 9

MAX1993 DYNAMIC OUTPUT VOLTAGE TRANSITION (C_{REFIN} = 100pF)



A. V_{GATE} = 0 TO 5V; 5V/div
B. OUTPUT = 1.5V TO 1.0V; 0.5V/div
C. V_{REFIN}: 0.5V/div
D. PGOOD: 5V/div
E. INDUCTOR CURRENT: 2.5A/div
100mA LOAD, $\overline{SKIP}$ = GND, CIRCUIT OF FIGURE 9

Pin Description

PIN		NAME	FUNCTION
MAX1992	MAX1993		
1	1	TON	On-Time Selection Control Input. This four-level logic input sets the K-factor value used to determine the DH on-time (see the *On-Time One-Shot* section). Connect to analog ground (AGND or GND), REF, V_{CC}, or leave TON unconnected to select the following nominal switching frequencies: V_{CC} = 200kHz Open = 300kHz REF = 450kHz AGND = 600kHz
2, 7, 8	—	N.C.	No Connection. Not internally connected.
—	2	FBLANK	Fault Blanking Control Input. This four-level logic input enables or disables fault blanking, and sets the minimum forced-PWM operation time (t_{FBLANK}). When fault blanking is enabled, PGOOD, OVP protection, and UVP protection are blanked for the selected time period after a transition is detected on GATE. Additionally, the controller enters forced-PWM mode for the duration of t_{FBLANK} anytime GATE changes states. Connect FBLANK as follows: V_{CC} = 140µs (min) t_{FBLANK}, fault blanking enabled Open = 90µs (min) t_{FBLANK}, fault blanking enabled REF = 40µs (min) t_{FBLANK}, fault blanking enabled AGND = 90µs (min) t_{FBLANK}, fault blanking disabled

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1992	MAX1993		
3	3	LSAT	Inductor Saturation Control Input. This four-level logic input sets the inductor current saturation limit as a multiple of the valley current-limit threshold set by ILIM, or disables the function if not required. Connect LSAT to the following pins to set the saturation current limit: V_{CC} = 2 × $I_{LIM(VAL)}$ Open = 1.75 × $I_{LIM(VAL)}$ REF = 1.5 × $I_{LIM(VAL)}$ AGND = disable LSAT protection See the *Inductor Saturation Limit* and *Setting the Current Limit* sections.
4	4	PGOOD	Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 10% (typ) above or below the normal regulation point, during soft-start, and in shutdown. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation. For the MAX1993, PGOOD is blanked—forced high-impedance state—when FBLANK is enabled and the controller detects a transition on GATE.
5	5	ILIM	Valley Current-Limit Threshold Adjustment. The valley current-limit threshold defaults to 50mV if ILIM is tied to V_{CC}. In adjustable mode, the valley current-limit threshold across CSP and CSN is precisely 1/10th the voltage seen at ILIM over a 250mV to 2.5V range. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V. When the inductor saturation protection threshold is exceeded, ILIM sinks 6µA. See the *Current-Limit Protection (ILIM)* section.
6	6	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.1µF or greater ceramic capacitor. The reference can source up to 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error. The reference is disabled when the MAX1992/MAX1993 is shut down.
—	7	REFIN	External Reference Input. REFIN sets the feedback regulation voltage (V_{FB} = V_{REFIN}) of the MAX1993.
—	8	OD	Open-Drain Output. Controlled by GATE.
9	9	FB	Feedback Input. MAX1992: Connect to V_{CC} for a +1.8V fixed output or to AGND for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB to a resistive divider from the output voltage. The FB regulation level is +0.7V. MAX1993: The FB regulation level is set by the voltage at REFIN.
10	10	OUT	Output Voltage Sense. Connect directly to the positive terminal of the output capacitors as shown in the standard application circuits (Figures 1 and 9). OUT senses the output voltage to determine the on-time for the high-side switching MOSFET. For the MAX1992, OUT also serves as the feedback input when using the preset internal output voltages as shown in Figure 7. When discharge mode is enabled by OVP/UVP, the output capacitor is discharged through an internal 10Ω resistor connected between OUT and ground.
11	11	CSP	Positive Current-Sense Input. Connect to the positive terminal of the current-sense element. Figure 10 and Table 7 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1992	MAX1993		
12	12	CSN	Negative Current-Sense Input. Connect to the negative terminal of the current-sense element. Figure 10 and Table 7 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM.
13	13	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect $\overline{SKIP}$ to V_{CC} for low-noise, forced-PWM mode or connect $\overline{SKIP}$ to analog ground (AGND or GND) to enable pulse-skipping operation.
14	14	V+	Battery Voltage-Sense Connection. The controller only uses V+ to set the on-time one-shot timing. The DH on-time is inversely proportional to input voltage over a range of 2V to 28V.
15	15	DH	High-Side Gate-Driver Output. DH swings from LX to BST.
16	16	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
17	17	BST	Boost Flying Capacitor Connection. Connect to an external capacitor and diode as shown in Figure 6. An optional resistor in series with BST allows the DH pullup current to be adjusted.
18	18	DL	Low-Side Gate-Driver Output. DL swings from PGND to V_{DD} (MAX1992) or GND to V_{DD} (MAX1993).
19	19	V_{DD}	Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to PGND with a 1µF or greater ceramic capacitor.
20	—	PGND	Power Ground. Ground connection for the DL low-side gate driver.
—	20	GND	Analog and Power Ground. AGND and PGND connect together internally. Connect backside pad to GND.
21	—	AGND	Analog Ground. Connect backside pad to AGND.
—	21	GATE	Buffered N-Channel MOSFET Gate Input. A logic low on GATE turns off the internal MOSFET so OD appears as a high impedance. A logic high on GATE turns on the internal MOSFET, pulling OD to ground.
22	22	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 20Ω resistor. Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1992	MAX1993		
23	23	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to analog ground to put the controller into its 1µA shutdown state. When discharge mode is enabled by OVP/UVP, the output is discharged through a 10Ω resistor between OUT and ground, and DL is forced high after V_{OUT} drops below 0.3V. When discharge mode is disabled by OVP/UVP, OUT remains a high-impedance input and DL is forced low, so LX also appears as a high-impedance input. A rising edge on $\overline{SHDN}$ clears the fault-protection latch.
24	24	OVP/UVP	Overvoltage/Undervoltage Protection and Discharge Mode Control Input. This four-level logic input selects between various output fault-protection options (Table 6) by selectively enabling OVP protection and UVP protection. When enabled, the OVP limit defaults at 116% of the nominal output voltage, and the UVP limit defaults at 70% of the nominal output voltage. Discharge mode is enabled when UVP protection is also enabled. Connect OVP/UVP to the following pins for the desired function: V_{CC} = enable OVP and discharge mode, enable UVP Open = enable OVP and discharge mode, disable UVP REF = disable OVP and discharge mode, enable UVP AGND = disable OVP and discharge mode, and UVP See the *Fault Protection* and *Shutdown and Output Discharge* sections.

Table 1. Component Selection for Standard Applications

COMPONENT	V_{OUT} = 2.5V AT 5A (FIGURE 1)	V_{OUT} = 1.8V AT 5A	V_{OUT} = 1.0V / 1.5V AT 4A (FIGURE 9)
	V_{IN} = 7V to 24V, TON = OPEN (300kHz)	V_{IN} = 7V to 24V, TON = OPEN (300kHz)	V_{IN} = 4.5V to 5.5V, TON = GND (600kHz)
MAX1992	FB = AGND	FB = V_{CC}	Not recommended
MAX1993	Adjustable FB, REFIN = REF	FB = OUT, V_{REFIN} = 1.8V	FB = OUT, V_{REFIN} = 1.0V / 1.5V
C_{IN}, input capacitor	10µF, 25V Taiyo Yuden TMK432BJ106KM	10µF, 25V Taiyo Yuden TMK432BJ106KM	100µF, 10V Sanyo POSCAP 10TPA100M
C_{OUT}, output capacitor	220µF, 4V, 15mΩ Sanyo POSCAP 4TPE220MF	220µF, 4V, 15mΩ Sanyo POSCAP 4TPE220MF	220µF, 6V, 12mΩ Sanyo POSCAP 6TPD220M
N_H high-side MOSFET	Fairchild Semiconductor 1/2 FDS6982A	Fairchild Semiconductor 1/2 FDS6982A	Fairchild Semiconductor 1/2 FDS6982S
N_L low-side MOSFET	Fairchild Semiconductor 1/2 FDS6982A	Fairchild Semiconductor 1/2 FDS6982A	Fairchild Semiconductor 1/2 FDS6982S
D_L Schottky rectifier (optional)	Nihon EP10QS03L 1A, 30V, 0.45Vf	Nihon EP10QS03L 1A, 30V, 0.45Vf	Nihon EP10QS03L 1A, 30V, 0.45Vf
L1 inductor	4.3µH Sumida CDEP105(L)	3.2µH Sumida CDEP105(L)	1.4µH Sumida CDEP105(L)
R_{SENSE}	15mΩ ±1% 0.5W resistor IRC LR2010-01-R015F or Dale WSL-2010-R015F	15mΩ ±1% 0.5W resistor IRC LR2010-01-R015F or Dale WSL-2010-R015F	15mΩ ±1% 0.5W resistor IRC LR2010-01-R015F or Dale WSL-2010-R015F

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	714-373-7366 (USA)	www.panasonic.com
Sanyo	65-231-3226 (Singapore) 408-749-9714 (USA)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	03-3667-3408 (Japan) 408-573-4150 (USA)	www.t-yuden.com
TDK	847-803-6100 (USA) 81-3-5201-7241 (Japan)	www.component.tdk.com
TOKO	858-675-8013 (USA)	www.tokoam.com

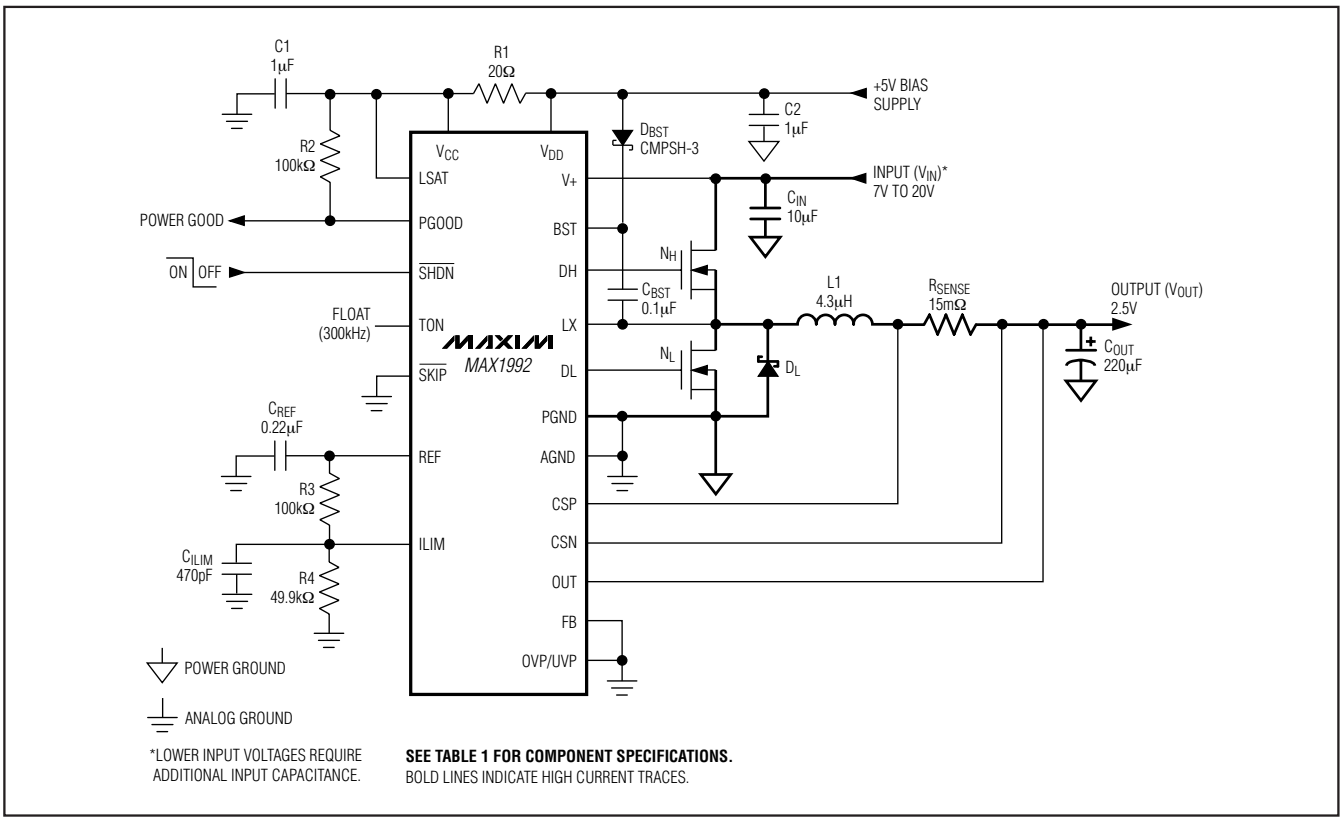


Figure 1. MAX1992 Standard Application Circuit

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Detailed Description

The MAX1992/MAX1993 buck controllers are ideal for low-voltage power supplies for notebook computers. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX1992/MAX1993 is designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

See Table 1 for component selections and Table 2 for a list of component suppliers.

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1992/MAX1993 require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 2mA \text{ to } 20mA \text{ (typ)}$$

where I_{CC} is 550µA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

The V+ battery input and 5V bias inputs (V_{CC} and V_{DD}) can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present in order to ensure startup.

Free-Running Constant-On-Time PWM Controller with Input Feed Forward

The Quick-PWM control architecture is a pseudofixed-frequency, constant on-time, current-mode regulator with voltage feed forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input and is proportional to the output voltage:

$$\text{On-time} = K (V_{OUT} + 0.075V) / V_{IN}$$

Table 3. Approximate K-Factor Errors

TON SETTING (kHz)	TYPICAL K-FACTOR (µs)	K-FACTOR ERROR (%)	MINIMUM V_{IN} AT V_{OUT} = 2.5V (h = 1.5) (V)	TYPICAL APPLICATION	COMMENTS
200 (TON = V_{CC})	5.0	±10	3.14	4-cell Li+ notebook	Use for absolute best efficiency
300 (TON = open)	3.3	±10	3.47	4-cell Li+ notebook	Considered mainstream by current standards
450 (TON = REF)	2.2	±12.5	4.13	3-cell Li+ notebook	Useful in 3-cell systems for lighter loads than the CPU core or where size is key
600 (TON = GND)	1.7	±12.5	5.61	+5V input	Good operating point for compound buck designs or desktop circuits

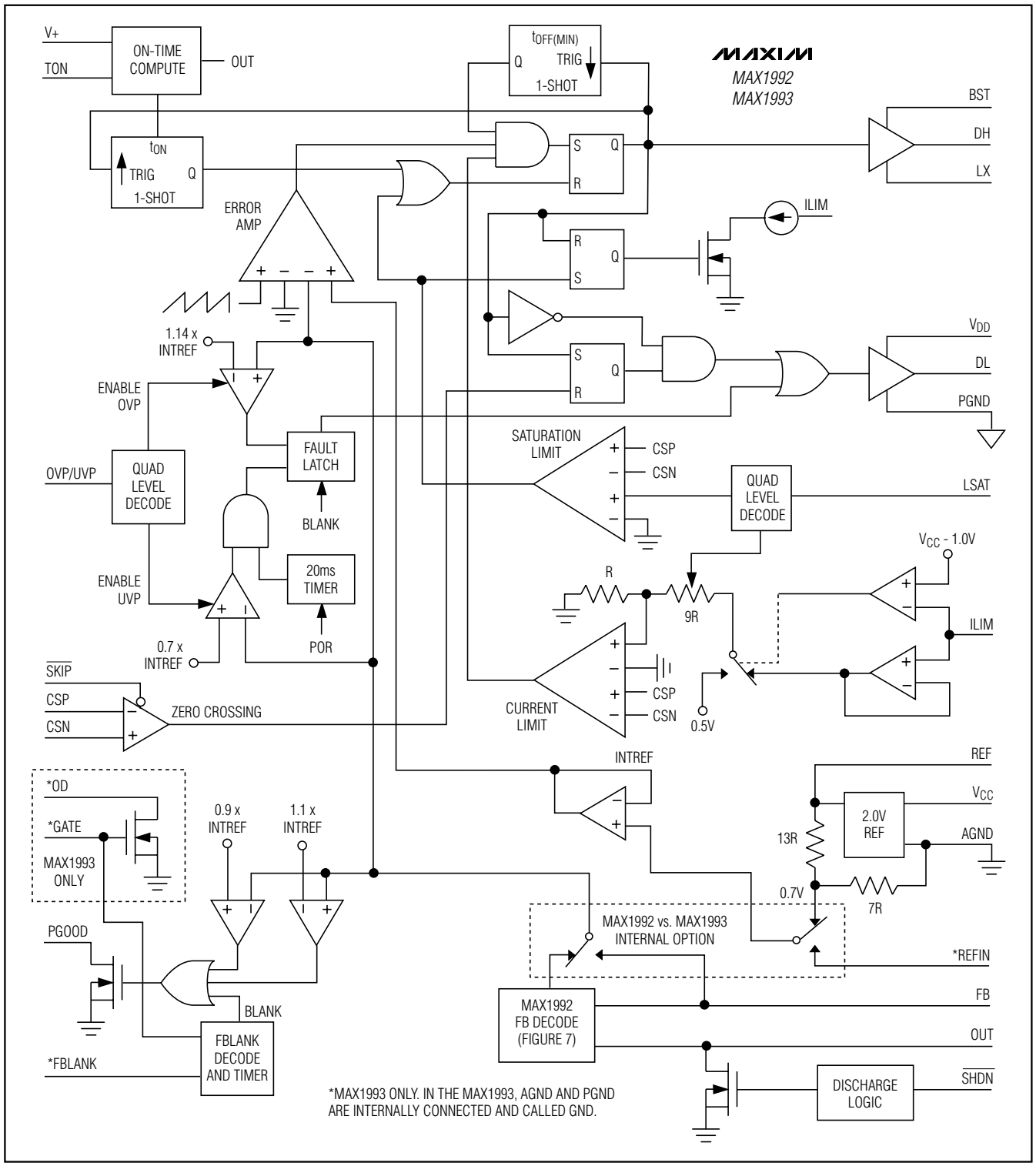


Figure 2. MAX1992/MAX1993 Functional Diagram

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

where K (switching period) is set by the TON pin-strap connection (Table 3), and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: 1) the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; 2) the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* (approximately ±12.5% at 600kHz and 450kHz and ±10% at 200kHz and 300kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range. For example, the 600kHz setting typically runs approximately 10% slower with inputs much greater than 5V due to the very short on-times required.

The constant on-time translates only roughly to a constant switching frequency. The on-times guaranteed in the *Electrical Characteristics* are influenced by resistive losses and by switching delays in the high-side MOSFET. Resistive losses—including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground—tend to raise the switching frequency as the load increases. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times are added to the effective on-time. It occurs only in PWM mode ($\overline{SKIP}$ = V_{CC}) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT} + V_{DROP1}}{t_{ON}\left(V_{IN} + V_{DROP2}\right)}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, including the high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX1992/MAX1993.

Automatic Pulse-Skipping Mode ($\overline{SKIP}$ = GND)

In skip mode ($\overline{SKIP}$ = GND), an inherent automatic switchover to PFM takes place at light loads (Figure 3). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the current-sense resistor (CSP to CSN). Once V_{CSP} - V_{CSN} drops below 5% of the current-limit threshold (2.5mV for the default 50mV current-limit threshold), the comparator forces DL low (Figure 2). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to one-half the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). This threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} \approx \left(\frac{V_{OUT}K}{2L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where K is the on-time scale factor (Table 3). For example, in the standard application circuit (K = 3.3µs, V_{OUT} = 2.5V, V_{IN} = 12V, and L = 4.3µH), the pulse-skipping switchover occurs at:

$$\left(\frac{2.5V \times 3.3\mu s}{2 \times 4.3\mu H}\right)\left(\frac{12V - 2.5V}{12V}\right) = 0.76A$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used. The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

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DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX1992/MAX1993 regulate the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($\overline{SKIP}$ = GND and $I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% because of slope compensation.

Forced-PWM Mode ($\overline{SKIP}$ = VCC)

The low-noise forced-PWM mode ($\overline{SKIP}$ = V_{CC}) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of V_{OUT}/V_{IN}. Forced-PWM mode keeps the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 2mA and 20mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment. The MAX1993 uses forced-PWM operation during all dynamic output voltage transitions (GATE transition detected) in order to ensure fast, accurate transitions. Because forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads, quickly discharging the output capacitors. FBLANK determines how long the MAX1993 maintains forced-PWM operation—140µs (FBLANK = V_{CC}), 90µs (FBLANK = open or AGND), or 40µs (FBLANK = REF).

Current-Limit Protection (ILIM)

Valley Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses a current-sense resistor between CSP and CSN as the current-sensing element (Figure 10). If the magnitude of the current-sense signal is above the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle (Figure 5). The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

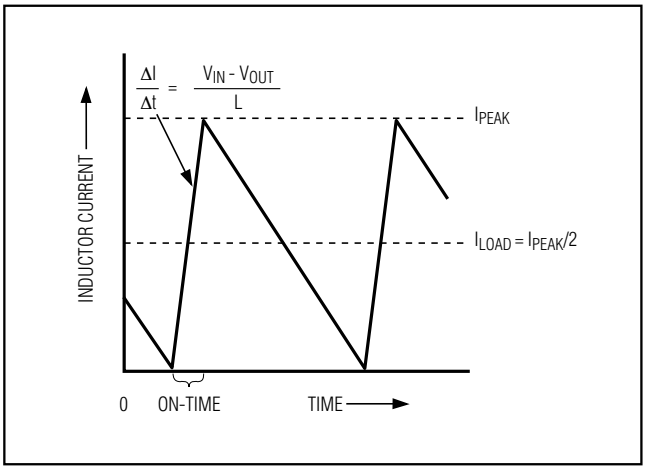

Figure 3. Pulse-Skipping/Discontinuous Crossover Point

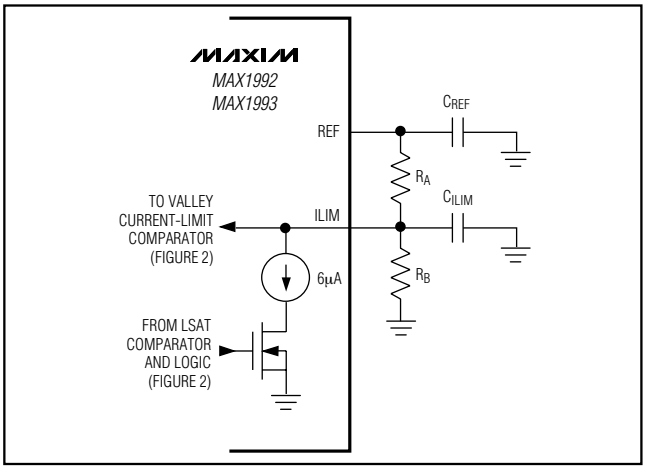

Figure 4. Adjustable Current-Limit Threshold

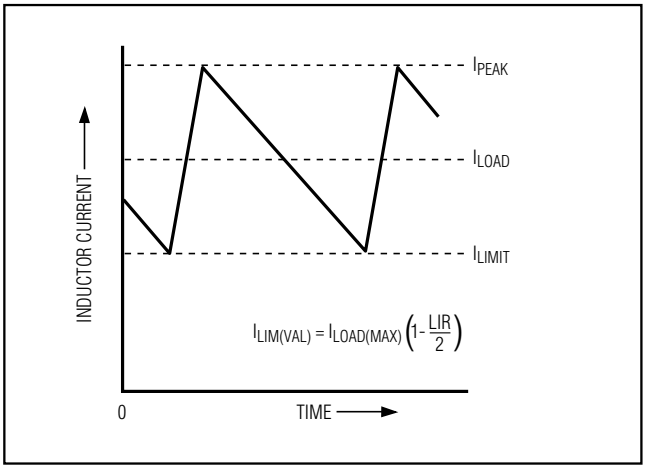

Figure 5. "Valley" Current-Limit Threshold Point

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

In forced-PWM mode, the MAX1992/MAX1993 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. A 2µA to 20µA divider current is recommended for accuracy and noise immunity. The current-limit threshold adjustment range is from 25mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 50mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSP and CSN. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Inductor Saturation Limit

The LSAT connection selects an upper current-sense limit as the inductor saturation threshold or disables the inductor saturation protection feature altogether (LSAT = GND). When enabled, the inductor saturation threshold is set as a multiple of the positive valley current-limit threshold (Table 4) and tracks the valley current limit when ILIM is adjusted. The inductor saturation threshold should be selected to give sufficient headroom above the peak inductor current so switching noise does not accidentally trip the saturation protection. Selecting too high a threshold can cause an inductor saturation to go undetected. For an inductor with a low LIR (the ratio of the inductor ripple current to the designed maximum load current) of approximately 20%, the lowest saturation threshold of 1.5 x $I_{LIM(VAL)}$ (LSAT = REF) may be acceptable. When using an inductor with a higher LIR, increase the inductor saturation threshold accordingly.

When inductor saturation is enabled, the MAX1992/MAX1993 continuously monitor the inductor current through the voltage across the current-sense resistor. When the inductor saturation threshold is exceeded, the MAX1992/MAX1993 immediately turn off the high-side gate driver and enable a 6µA discharge current on ILIM (Figure 4) at the beginning of the next DH on-time.

This reduces the voltage on ILIM by ΔV_{ILIM} where:

$$\Delta V_{ILIM} = -\left(\frac{R_A \times R_B}{R_A + R_B}\right) I_{ILIM(LSAT)}$$

where $I_{ILIM(LSAT)}$ is 6µA ILIM saturation fault sink current (see the *Electrical Characteristics* table). When using the default 50mV valley current-limit threshold (ILIM = V_{CC}), the ILIM saturation fault sink current does not lower the current-limit threshold (see Figure 2).

If the inductor current remains below the saturation threshold during the next cycle, the ILIM discharge current is disabled, and the ILIM voltage returns to its original set point. The inductor should not remain in saturation once the controller reduces the valley current limit. However, if the inductor remains in saturation, the output voltage may drop low enough to trip the undervoltage fault protection (UVP enabled), causing the MAX1992/MAX1993 to shut down and latch off. Adding a capacitor from ILIM to GND slows the ILIM voltage change by the time constant $\tau = (R_A // R_B) \times C_{ILIM}$. A suitable time constant is between 5 to 10 switching cycles. If the inductor saturation occurs only during a short load transient, the time constant allows the power supply to recover before the output voltage drops below the output undervoltage threshold.

Set ΔV_{ILIM} to be at least 30% (LIR) of the ILIM set voltage. Calculate R_A and R_B using the equations below:

$$R_A = \frac{V_{REF}}{I_{ILIM(LSAT)}}\left(\frac{\Delta V_{ILIM}}{V_{ILIM(SET)}}\right)$$

$$\text{with}\left(\frac{\Delta V_{ILIM}}{V_{ILIM(SET)}}\right) \text{ set at 30\%}$$

$$R_B = \frac{R_A}{\left(\frac{V_{REF}}{V_{ILIM(SET)}} - 1\right)}$$

Inductor saturation works best using a current-sense resistor in series with the inductor. A low-side current-sense resistor configuration can sense the saturation

Table 4. LSAT Configuration Table

LSAT	INDUCTOR SATURATION THRESHOLD
V_{CC}	2.00 × $I_{LIM(VAL)}$
Open	1.75 × $I_{LIM(VAL)}$
REF	1.50 × $I_{LIM(VAL)}$
GND	Disabled

current only at the start of the off-cycle. See *Setting the Current Limit* section for various current-sense configurations (Figure 10) and LSAT recommendations.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is off. A similar adaptive dead-time circuit monitors the DH output, preventing the low-side MOSFET from turning on until DH is off. There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates in order for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX1992/MAX1993 interpret the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL from being pulled up because of capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high-input voltages and long inductive driver traces can require additional gate-to-source capacitance to ensure that fast-rising LX edges do not pull up the low-side MOSFETs gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold.

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Alternatively, adding a resistor of less than 10Ω in series with BST can remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 6).

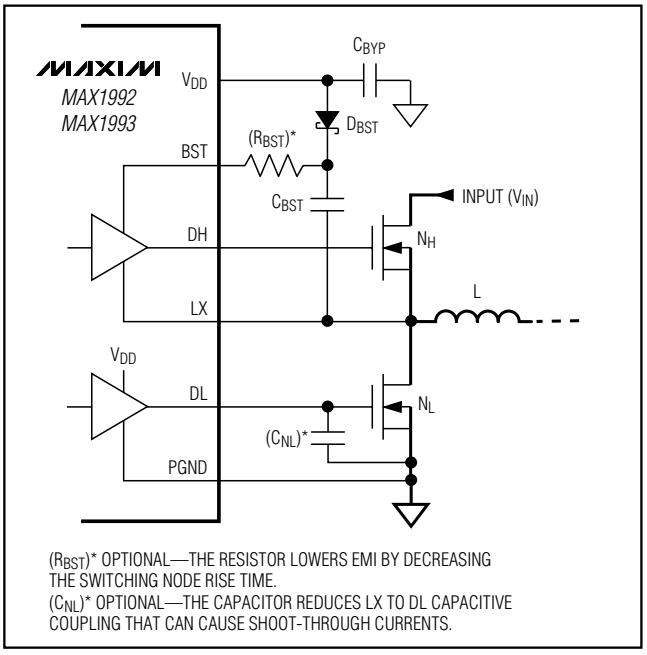

Figure 6. Optional Gate Driver Circuitry

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, powering up the reference, and preparing the PWM for operation. Until V_{CC} reaches 4.25V (typ), V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching. The controller inhibits switching by pulling DH low and holding DL low when OVP and shutdown discharge are disabled or forcing DL high when OVP and shutdown discharge are enabled (Table 6). When V_{CC} rises above 4.25V, the controller activates the PWM controller and initializes soft-start.

Soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge currents. The MAX1992/MAX1993 divide the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach regulation within 425µs, soft-start enters the second phase, and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached after 1.7ms or when the output reaches the nominal regulation voltage, whichever occurs first (see soft-start waveforms in the *Typical Operating Characteristics*). Adding a capacitor in parallel with the external ILIM resistors creates a continuously adjustable analog soft-start function.

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Power-Good Output (PGOOD)

PGOOD is the open-drain output for a window comparator that continuously monitors the output. PGOOD is actively held low in shutdown and during soft-start. After the digital soft-start terminates, PGOOD becomes high impedance as long as the output voltage is within ±10% of the nominal regulation voltage set by FB. When the output voltage drops 10% below or rises 10% above the nominal regulation voltage, the MAX1992/MAX1993 pull PGOOD low. Any fault condition forces PGOOD low until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling V_{CC} power below 1V. For logic level output voltages, connect an external pullup resistor between PGOOD and V_{CC}. A 100kΩ resistor works well in most applications.

Note that the PGOOD window detector is completely independent of the overvoltage and undervoltage protection fault detectors.

Fault Blanking (MAX1993 FBLANK)

The MAX1993 automatically enters forced-PWM operation during all dynamic output voltage transitions (GATE transition detected) in order to ensure fast, accurate transitions. FBLANK determines how long the MAX1993 maintains forced-PWM operation (Table 5)—at least 140µs (FBLANK = V_{CC}), 90µs (FBLANK = open or GND), or 40µs (FBLANK = REF).

When fault blanking is enabled (FBLANK = V_{CC}, open, or REF), the MAX1993 also disables the overvoltage and undervoltage fault protection and forces PGOOD to a high-impedance state during the transition period selected by FBLANK (Table 5). This prevents fault protection from latching off the controller and the PGOOD signal from going low when the output voltage change (ΔV_{OUT}) cannot occur as fast as the REFIN voltage change (ΔV_{REFIN}).

Table 5. FBLANK Configuration Table

FBLANK	FAULT BLANKING	MINIMUM FORCED-PWM DURATION (µs)
V_{CC}	Enabled	140
Open	Enabled	90
REF	Enabled	40
GND	Disabled	90

Shutdown and Output Discharge

When output discharge is enabled (OVP/UVP = V_{CC} or open) and $\overline{SHDN}$ is pulled low, or the output undervoltage fault latch is set (OVP/UVP = V_{CC} or REF), the MAX1992/MAX1993 discharge the output through an internal 10Ω switch to ground. While the output is discharging, DL is forced low and the PWM controller is disabled, but the reference remains active to provide an accurate threshold. Once the output voltage drops below 0.3V, the MAX1992/MAX1993 shut down the reference and pull DL high, effectively clamping the output and LX switching node to ground.

When output discharge is disabled (OVP/UVP = REF or GND), the controller does not actively discharge the output, and the DL driver remains low. Under these conditions, the output discharge rate is determined by the load current and output capacitance.

The controller detects and latches the discharge mode state set by OVP/UVP on startup.

Fault Protection

The MAX1992/MAX1993 provide over/undervoltage fault protection. Drive OVP/UVP to enable and disable fault protection as shown in Table 6. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions.

Overvoltage Protection (OVP)

When the output voltage rises above 116% of the nominal regulation voltage and OVP is enabled (OVP/UVP = V_{CC} or open), the OVP circuit sets the fault latch, shuts down the PWM controller, and immediately pulls DH low and forces DL high. This turns on the synchronous rectifier MOSFET with 100% duty, rapidly discharging the output capacitor and clamping the output to ground. Note that immediately latching DL high can cause the output voltage to go slightly negative due to energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse blows. OVP is ignored when transitions are detected on GATE (MAX1993 only, FBLANK enabled). Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to clear the fault latch and restart the controller.

OVP is disabled when OVP/UVP is connected to REF or GND (Table 6).

Table 6. Fault Protection and Shutdown Setting Truth Table

OVP/UVP	$\overline{SHDN}$ DISCHARGE*	UVP PROTECTION	OVP PROTECTION	THERMAL PROTECTION
V_{CC}	Yes. DL forced high when shut down.	Enabled. Discharge sequence activated; DL forced high when shut down.	Enabled. DH pulled low and DL forced high.	Enabled. Discharge sequence activated; DL forced high when shut down.
Open	Yes. DL forced high when shut down.	Disabled.	Enabled. DH pulled low and DL forced high.	Enabled. Discharge sequence activated; DL forced high when shut down.
REF	No. DL forced low when shut down.	Enabled. Discharge sequence activated; DL forced high when shut down.	Disabled.	Enabled. Discharge sequence activated; DL forced high when shut down.
GND	No. DL forced low when shut down.	Disabled.	Disabled.	Enabled. Discharge sequence activated; DL forced high when shut down.

**Discharge-mode state latched on power-up.*

Undervoltage Protection (UVP)

When the output voltage drops below 70%, the nominal regulation voltage and the UVP are enabled (OVP/UVP = V_{CC} or REF), and the controller sets the fault latch and begins the discharge mode (see the *Shutdown and Output Discharge* section). When the output voltage drops to 0.3V, the synchronous rectifiers turn on, clamping the outputs to GND. UVP is ignored for at least 10ms (min) after startup ($\overline{SHDN}$ rising edge) and when transitions are detected on GATE (MAX1993 only, FBLANK enabled). Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to clear the fault latch and restart the controller.

UVP is disabled when OVP/UVP is left open or connected to GND (Table 6).

Thermal Fault Protection

The MAX1992/MAX1993 feature a thermal fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down using discharge mode regardless of the OVP/UVP setting. Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to reactivate the controller after the junction temperature cools by 15°C.

Output Voltage

Preset Output Voltages (MAX1992 Only)

The MAX1992's Dual Mode operation allows the selection of common voltages without requiring external components (Figure 7). Connect FB to AGND for a fixed 2.5V output, to V_{CC} for a fixed 1.8V output, or connect FB directly to OUT for a fixed 0.7V output.

Setting V_{OUT} with a Resistive Voltage-Divider at FB

The output voltage can be adjusted from 0.7V to 5.5V using a resistive voltage-divider (Figure 8). The MAX1992 regulates FB to a fixed reference voltage (0.7V). Alternatively, the MAX1993 regulates FB to the voltage set at REFIN, making the MAX1993 ideal for memory applications in which the termination supply must track the supply voltage. The adjusted output voltage is:

$$V_{OUT} = V_{FB}\left(1 + \frac{R_C}{R_D}\right)$$

where V_{FB} is 0.7V for the MAX1992 and $V_{FB} = V_{REFIN}$ for the MAX1993.

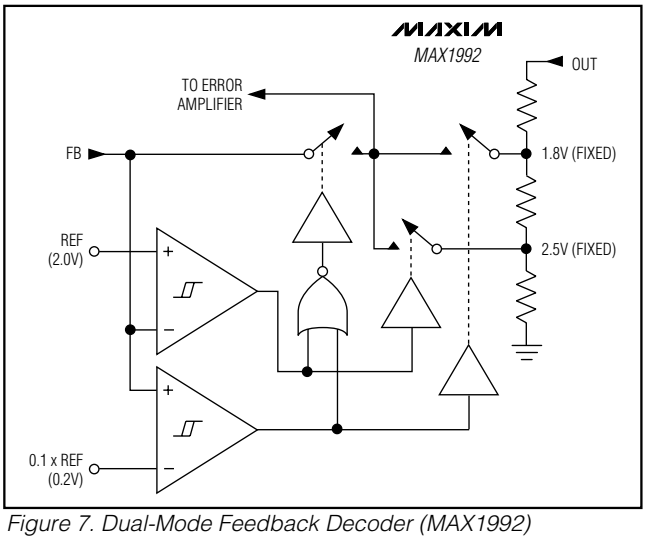

Figure 7. Dual-Mode Feedback Decoder (MAX1992)

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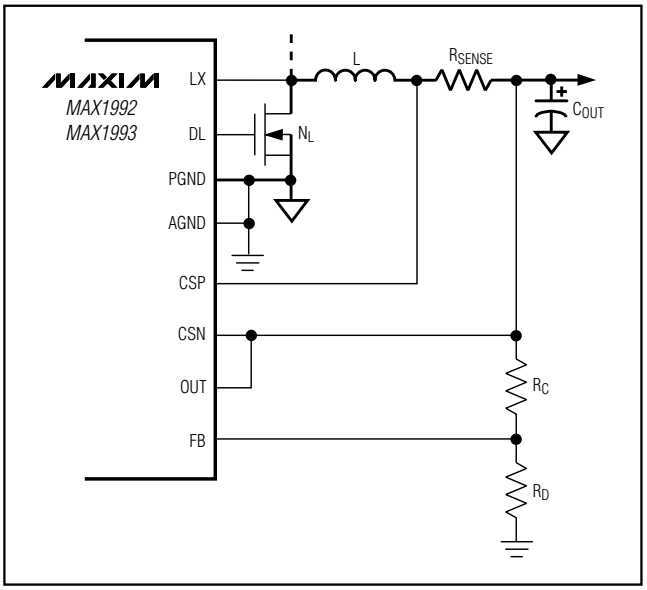

Figure 8. Setting V_{OUT} with a Resistive Voltage-Divider

Dynamic Output Voltages (MAX1993 Only)

The MAX1993 regulates FB to the voltage set at REFIN. By changing the voltage at REFIN, the MAX1993 can be used in applications that require dynamic output voltage changes between two set points. Figure 9 shows a dynamically adjustable resistive voltage-divider network at REFIN. Using the GATE signal and open-drain output (OD), a resistor can be switched in and out of the REFIN resistor-divider, changing the voltage at REFIN. A logic high on GATE turns on the internal N-channel MOSFET, forcing OD to a low-impedance state. A logic low on GATE disables the N-channel MOSFET, so OD is high impedance. The two output voltages (FB = OUT) are determined by the following equations:

$$V_{OUT(LOW)} = V_{REF}\left(\frac{R6}{R5+R6}\right)$$

$$V_{OUT(HIGH)} = V_{REF}\left[\frac{(R6+R7)}{R5+(R6+R7)}\right]$$

The MAX1993 automatically enters forced-PWM operation on the rising and falling edges of GATE and remains in forced-PWM mode for a minimum time selected by FBLANK (Table 5). Forced-PWM operation is required to ensure fast, accurate negative voltage transitions when REFIN is lowered. Because forced-PWM operation disables the zero-crossing comparator, the inductor current can reverse under light loads, quickly discharging the output capacitors. If fault blanking is enabled, the MAX1993 also disables the overvoltage and undervoltage fault protection and forces PGOOD to a high-impedance state for the period selected by FBLANK (Table 5).

For a step voltage change at REFIN, the rate of change of the output voltage is limited by the inductor current ramp, the total output capacitance, the current limit, and the load during the transition. The inductor current ramp is limited by the voltage across the inductor and the inductance. The total output capacitance determines how much current is needed to change the output voltage. Additional load current slows the output voltage change during a positive REFIN voltage change, and speeds the output voltage change during a negative REFIN voltage change. Increasing the current-limit setting speeds a positive output voltage change.

Adding a capacitor across REFIN and GND filters noise and controls the rate-of-change of the REFIN voltage during dynamic transitions. With the additional capacitance, the REFIN voltage slews between the two set points with a time constant determined by the equivalent parallel resistance seen by the slew capacitor (C_{REFIN}). Referring to Figure 9, the time constant for a positive REFIN voltage transition is:

$$\tau_{POS} = \left[\frac{R5\times(R6+R7)}{R5+(R6+R7)}\right]C_{REFIN}$$

and the time constant for a negative REFIN voltage transition is:

$$\tau_{NEG} = \left(\frac{R5\times R6}{R5+R6}\right)C_{REFIN}$$

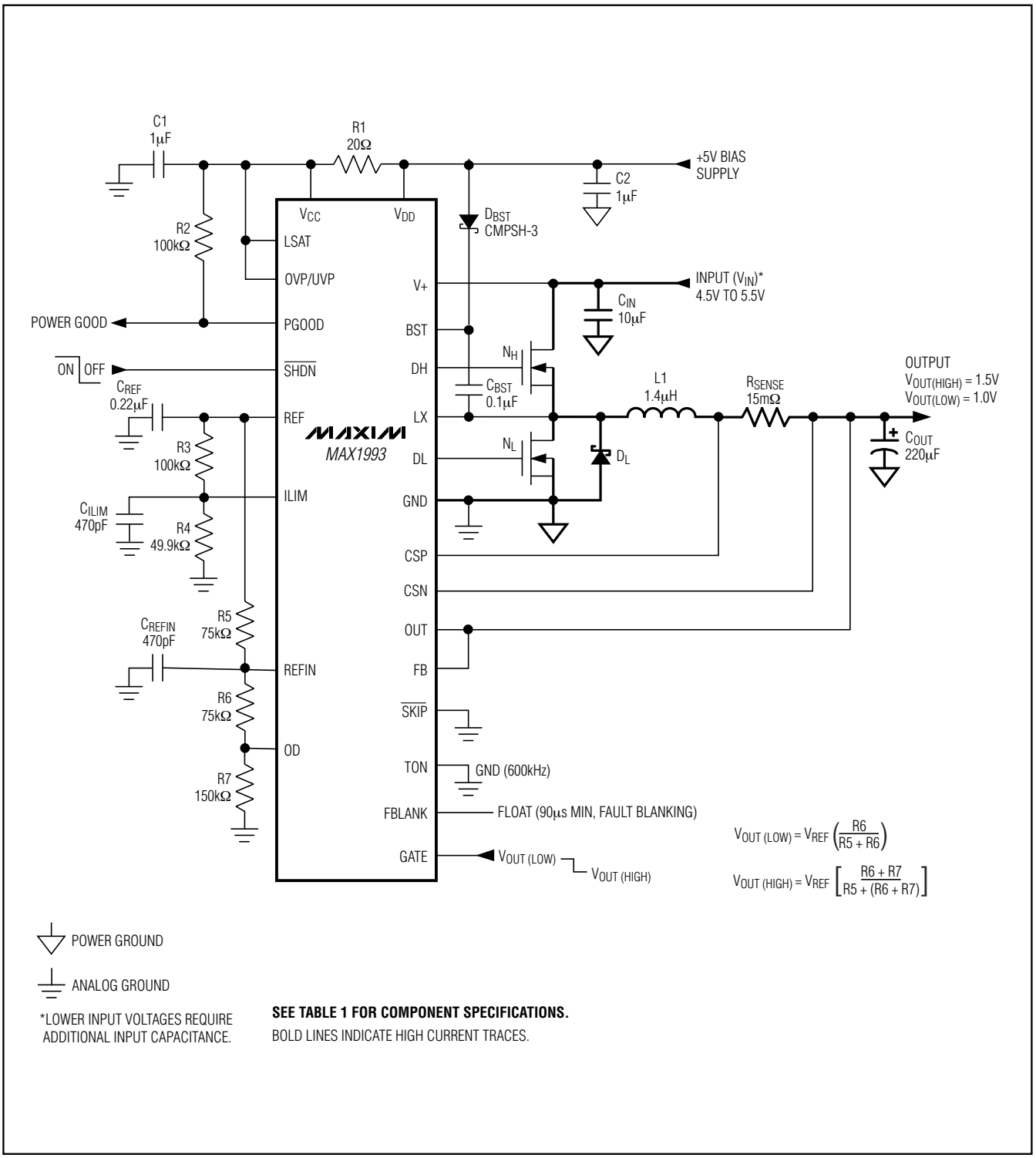

Figure 9. MAX1993 Standard Application Circuit

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range**. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice, lower input voltages result in better efficiency.
- **Maximum Load Current**. There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency**. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point**. This choice provides trade-offs: size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.3

$$L = \frac{2.5V(12V - 2.5)}{12V \times 300kHz \times 5A \times 0.3} = 4.40\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also affects transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2 \left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 3.

Table 7. Current-Sense Configurations

METHOD	CURRENT-SENSE ACCURACY	INDUCTOR SATURATION PROTECTION	CURRENT-SENSE POWER LOSS (EFFICIENCY)
A) Output Current-Sense Resistor	High	Allowed (highest accuracy)	$R_{SENSE} \times I_{OUT}^2$
B) Low-Side Current-Sense Resistor	High	Not allowed (LSAT = GND)	$\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{SENSE} \times I_{OUT}^2$
C) Low-Side MOSFET On-Resistance	Low	Not allowed (LSAT = GND)	No additional loss
D) Equivalent Inductor DC Resistance	Low	Allowed	No additional loss

The overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)}LIR}{2}\right)$$

where $I_{LIM(VAL)}$ equals the minimum valley current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). For the 50mV default setting, the minimum valley current-limit threshold is 40mV.

Connect ILIM to V_{CC} for a default 50mV valley current-limit threshold. In adjustable mode, the valley current-limit threshold is precisely 1/10th the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to analog ground (GND) with ILIM connected to the center tap. The external 250mV to 2V adjustment range corresponds to a 25mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the valley current-limit tolerance.

The current-sense method (Figure 10) and magnitude determine the achievable current-limit accuracy and power loss (Table 7). Typically, higher current-sense voltage limits provide tighter accuracy but also dissipate more power.

Most applications employ a valley current-sense voltage ($V_{LIM(VAL)}$) of 50mV to 100mV, so the sense resistor can be determined by:

$$R_{SENSE} = V_{LIM(VAL)} / I_{LIM(VAL)}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 10a. This configuration constantly monitors the inductor current, allowing accurate valley current-limiting and inductor saturation protection.

For low output voltage applications that require higher efficiency, the current-sense resistor can be connected between the source of the low-side MOSFET (N_L) and power ground (Figure 10b) with CSN connected to the drain of N_L and CSP connected to power ground. In this configuration, the additional current-sense resistance only dissipates power when N_L is conducting current. Inductor saturation protection must be disabled with this configuration (LSAT = GND) because the inductor current is only properly sensed when the low-side MOSFET is turned on.

For high-power applications that do not require high-accuracy current sensing or inductor saturation protection, the MAX1992/MAX1993 can use the low-side MOSFET's on-resistance as the current-sense element ($R_{SENSE} = R_{DS(ON)}$) by connecting CSN to the drain of N_L and CSP to the source of N_L (Figure 10c). Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise. Inductor saturation protection must be disabled with this configuration (LSAT = GND) because the inductor current is properly sensed only when the low-side MOSFET is turned on.

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

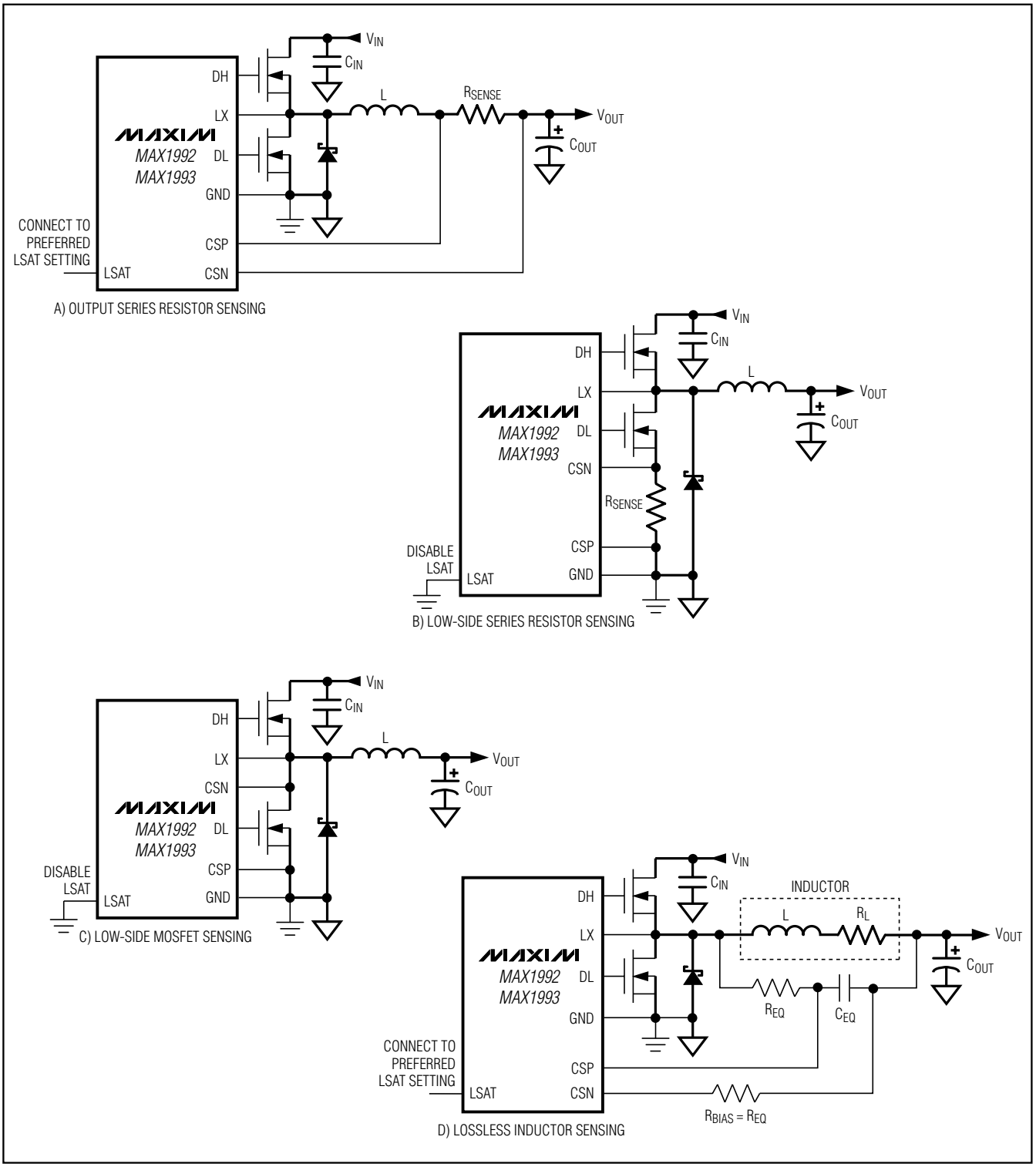

Figure 10. Current-Sense Configurations

Alternatively, high-power applications that require inductor saturation protection can constantly detect the inductor current by connecting a series RC circuit across the inductor (Figure 10d) with an equivalent time constant:

$$\frac{L}{R_L} = C_{EQ} \times R_{EQ}$$

where R_L is the inductor's series DC resistance. In this configuration, the current-sense resistance is equivalent to the inductor's DC resistance ($R_{SENSE} = R_L$). Use the worst-case inductance and R_L values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

In all cases, ensure an acceptable valley current-limit threshold voltage and inductor saturation configurations despite inaccuracies in sense resistance values.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications in which the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\Delta I_{LOAD(MAX)} LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OSCONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability (see the *Output Capacitor Stability Considerations* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OSCON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mV$_{P-P}$ ripple is 25mV/1.5A = 16.7mΩ. One 220µF/4V Sanyo polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired.

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Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1992/MAX1993 are operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX1992/MAX1993 DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD(N_H\,Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high-input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum efficiency occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H\,Switching) = \frac{(V_{IN(MAX)})^2 C_{RSS} f_{SW} I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$).

If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L) the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(N_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)}LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

Applications Information

Dropout Performance

The output voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases, unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{1 - \left(\frac{h \times t_{OFF(MIN)}}{K}\right)}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see the *On-Time One-Shot* (TON) section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

A dropout design example follows:

V_{OUT} = 2.5V

f_{SW} = 300kHz

K = 3.3µs, worst-case K_{MIN} = 3.0µs

$t_{OFF(MIN)}$ = 500ns

$V_{DROP1} = V_{DROP2}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = \left[\frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 500ns}{3.0\mu s}\right)}\right] + 0.1V - 0.1V = 3.47V$$

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

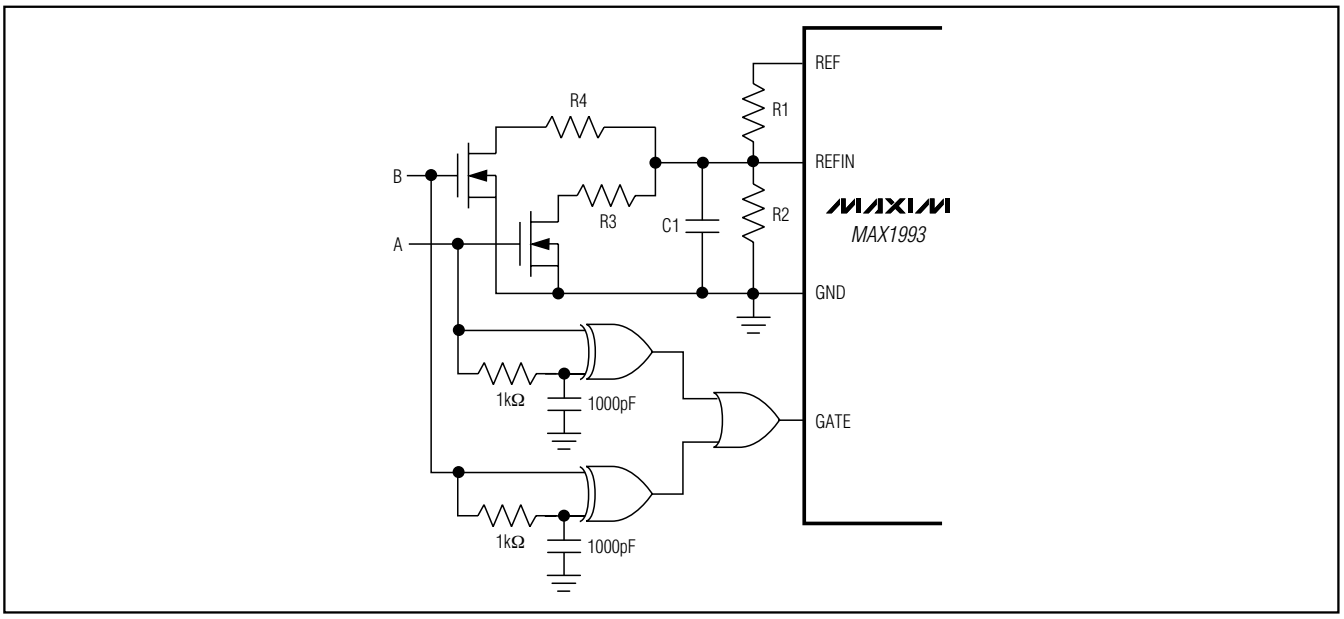


Figure 11. Multiple Output Voltage Settings

Calculating again with h = 1 and the typical K-factor value (K = 3.3µs) gives the absolute limit of dropout:

$$V_{IN(MIN)} = \left[\frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 500ns}{3.3\mu s}\right)}\right] + 0.1V - 0.1V = 3.06V$$

Therefore, V_{IN} must be greater than 3.06V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.47V.

Multiple Output Voltage Settings (MAX1993 Only)

While the MAX1993 is optimized to work with applications that require two dynamic output voltages, it can produce three or more output voltages if required by using discrete logic or a DAC.

Figure 11 shows an application circuit providing four voltage levels using discrete logic. Switching resistors in and out of the resistor network changes the voltage at REFIN. An edge detection circuit is added to generate a 1µs pulse on GATE to trigger the fault-blanking and forced-PWM operation. When using PWM mode ($\overline{SKIP}$ = V_{CC}), the edge detection circuit is only required if fault blanking is enabled. Otherwise, leave OD unconnected.

Active Bus Termination (MAX1993 Only)

Active bus termination power supplies generate a voltage rail that tracks a set reference. They are required to source and sink current. DDR memory architecture requires active bus termination. In DDR memory architecture, the termination voltage is set at exactly half the memory supply voltage. Configure the MAX1993 to generate the termination voltage using a resistor-divider at REFIN. In such an application, the MAX1993 must be kept in PWM mode ($\overline{SKIP}$ = V_{CC}) in order for it to source and sink current. Figure 12 shows the MAX1993 configured as a DDR termination regulator. Connect GATE and FBLANK to GND when unused.

Voltage Positioning

In applications where fast-load transients occur, the output voltage changes instantly by $ESR_{COUT} \times \Delta I_{LOAD}$. Voltage positioning allows the use of fewer output capacitors for such applications, and maximizes the output voltage AC and DC tolerance window in tight tolerance applications.

Figure 13 shows the connection of OUT and FB in a voltage-positioned circuit. In nonvoltage-positioned circuits, the MAX1992/MAX1993 regulate at the output capacitor. In voltage-positioned circuits, the MAX1992/MAX1993 regulate on the inductor side of the current-sense resistor. V_{OUT} is reduced to:

$$V_{OUT(VPS)} = V_{OUT(NO\ LOAD)} - R_{SENSE}I_{LOAD}$$

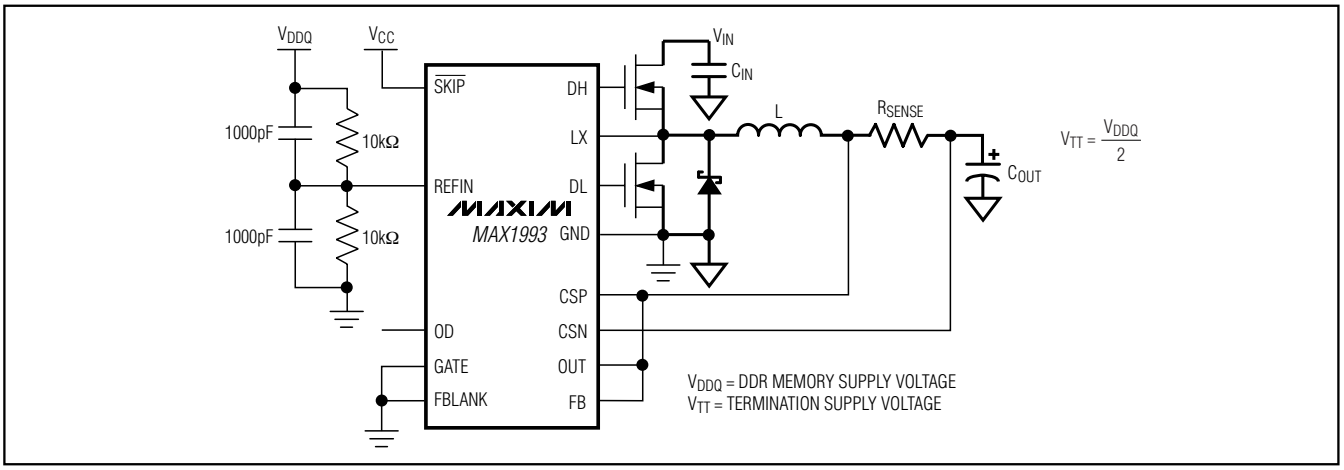


Figure 12. Active Bus Termination

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 15). If possible, mount all of the power components on the topside of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSP and CSN directly across the current-sense resistor (R_{SENSE}).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB, CSP, and CSN).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (N_L source, C_{IN}, C_{OUT}, and D_L anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the backside opposite N_L and N_H in order to keep LX, GND, DH, and the DL gate-drive lines short and wide. The DL and DH gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figures 1 and 9. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-to-DC converter circuit as close to the load as is practical.

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

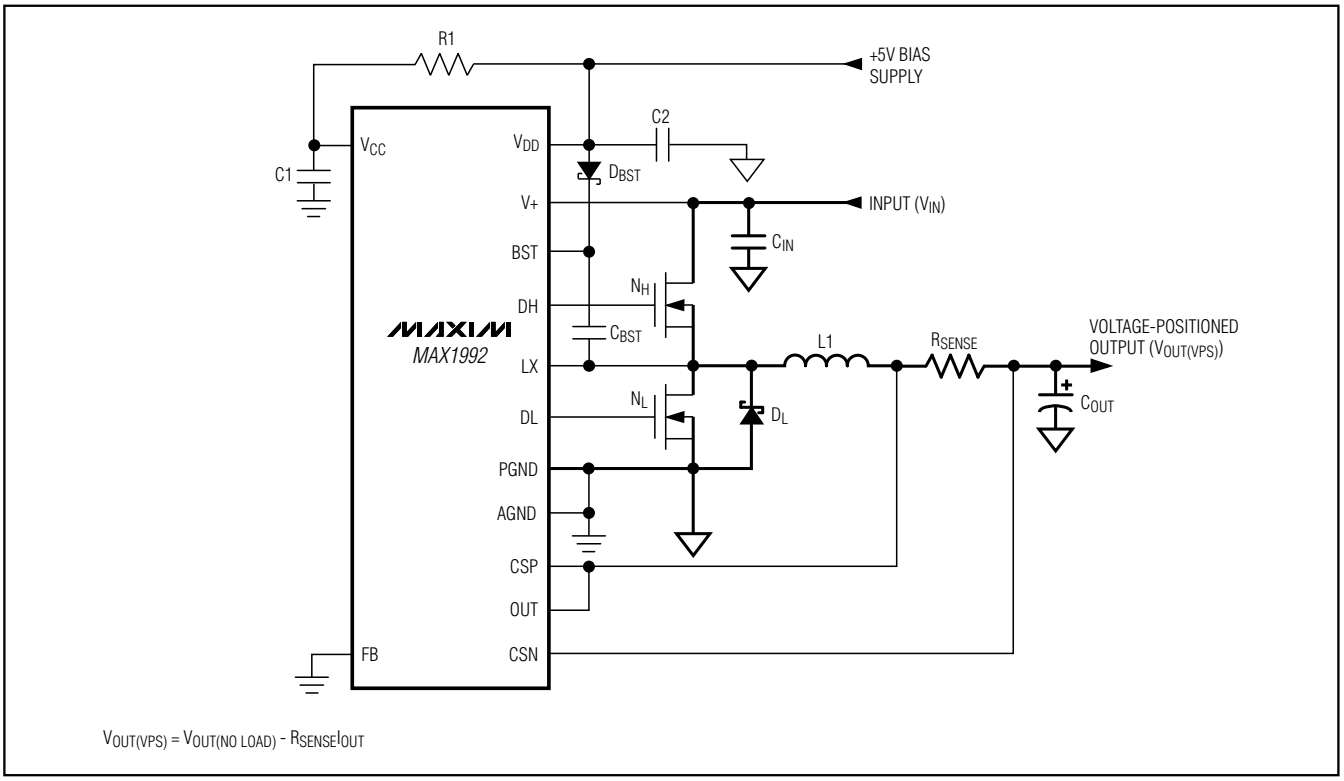


Figure 13. Voltage-Positioning Output

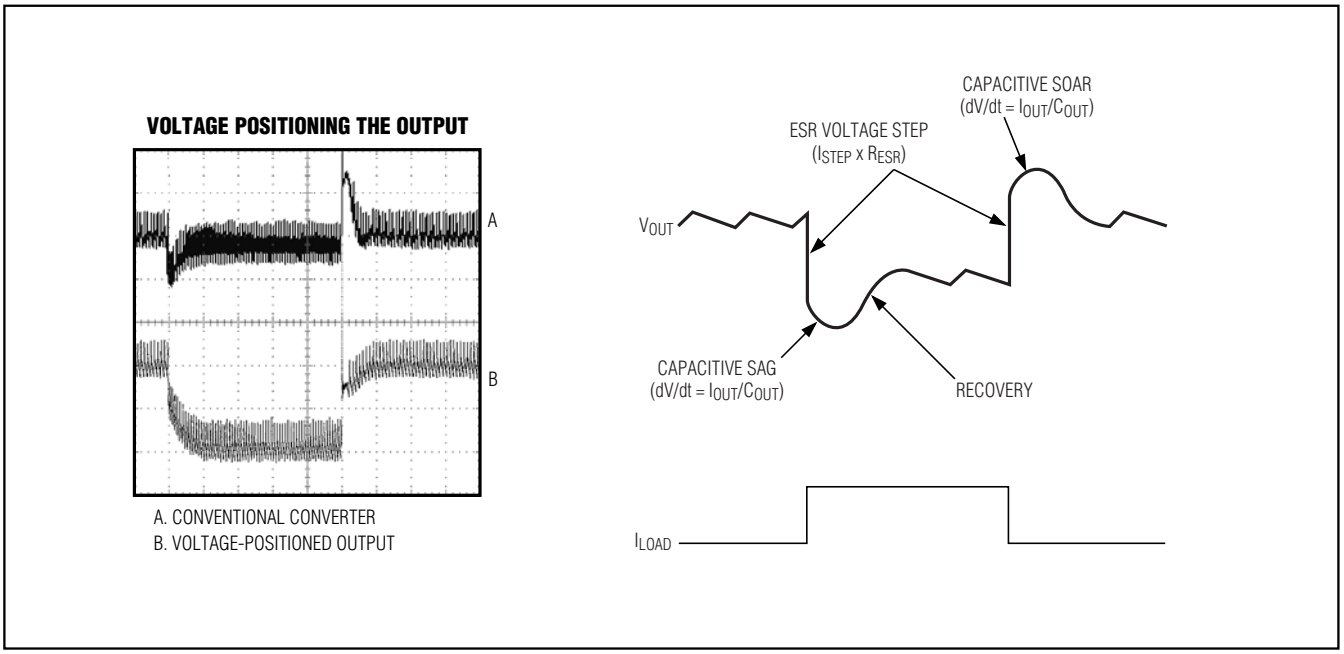


Figure 14. Voltage-Positioning Transient Response

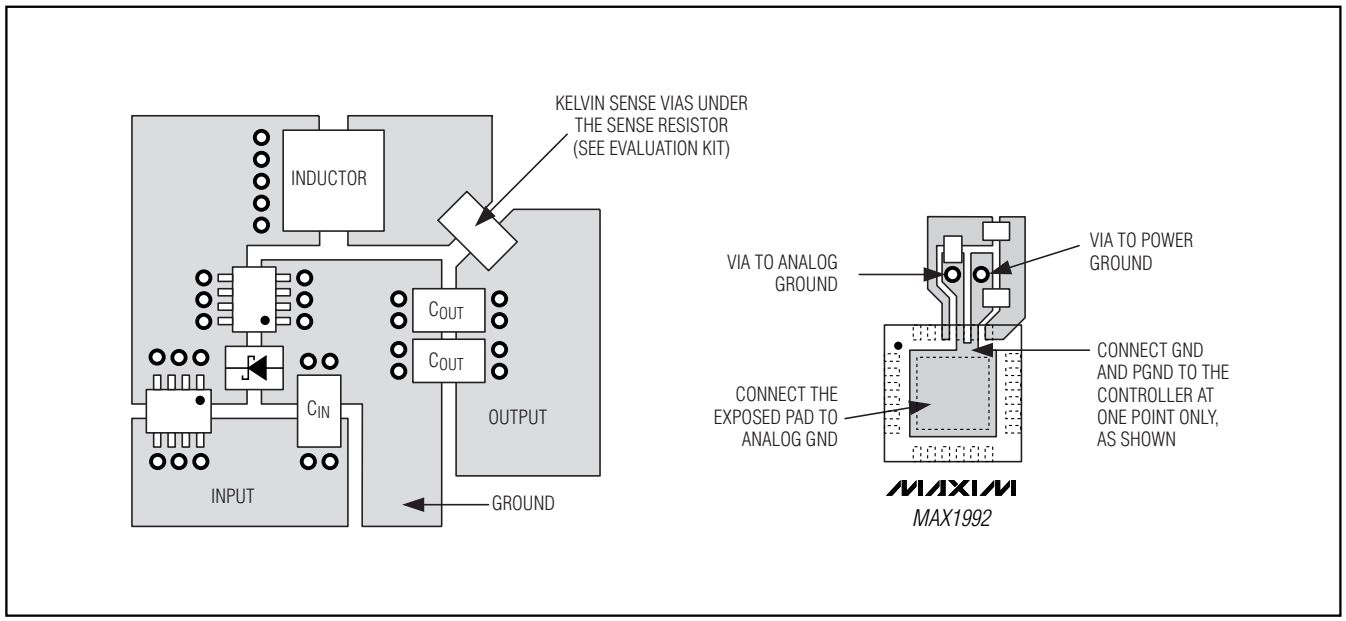
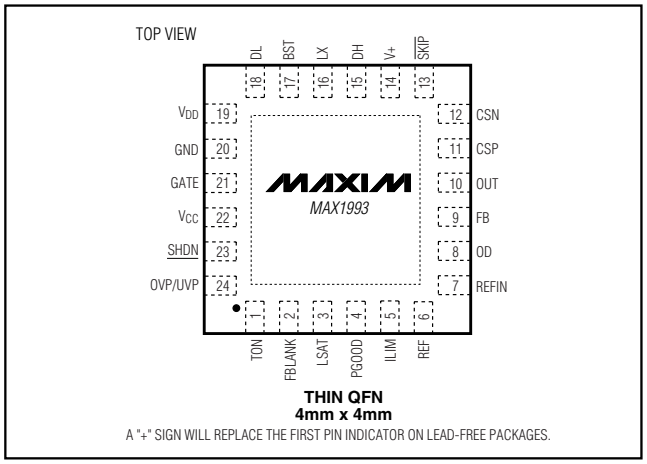


Figure 15. PC Board Layout

Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 2616

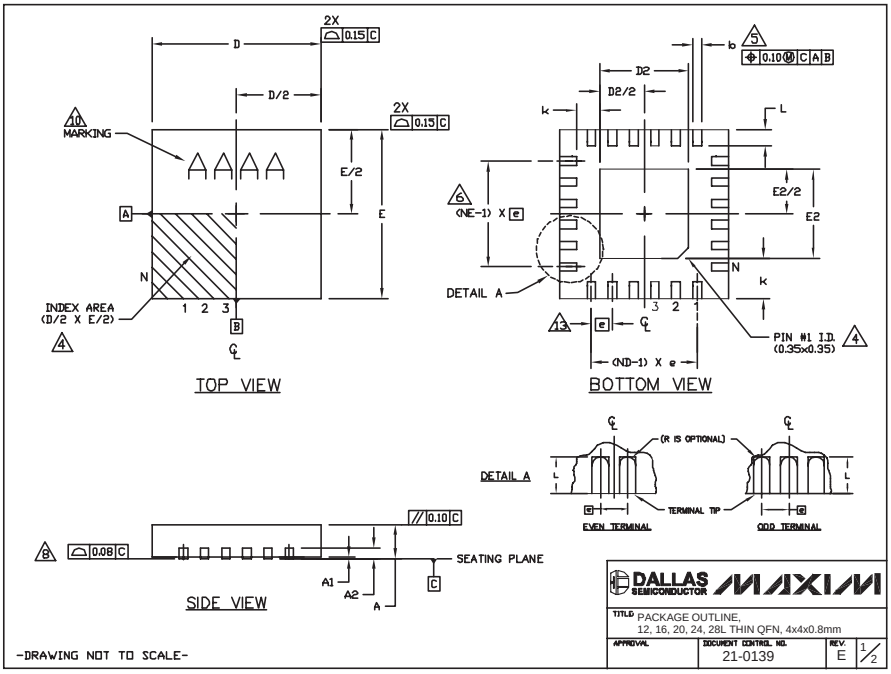
PROCESS: BiCMOS

Quick-PWM Step-Down Controllers with Inductor Saturation Protection and Dynamic Output Voltages

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGD			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. E
2/2